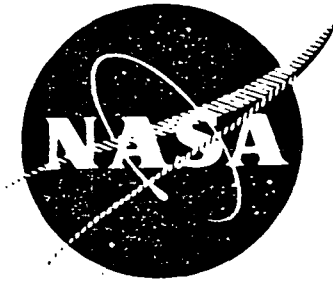


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DEVELOPMENT OF A
STANDARDIZED CONTROL MODULE
FOR
DC-TO-DC CONVERTERS

August 30, 1977

By:

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16. Abstract The electrical performance of a power processor depends, to a large extent, on the quality of its control system. Most of the existing control circuits suffer one or more of the following imperfections that tend to restrict their respective utility: (1) Inability to perform different modes of duty cycle control (2) Lack of immunity to output-filter parameter changes (3) Lack of capability to provide power-component stress limiting on an instantaneous basis. The three lagging aspects of existing control circuits in general have served to define the major objectives of the current Standardized Control Module (SCM) Program. The report presents detailed information on the SCM functional block diagram, its universality and performance features, circuit description, test results, and its modeling and analysis effort.					
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FOREWARD

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1. SUMMARY

Power processor control circuits in use today generally suffer at least one of the following limitations:

- (1) Unable to perform different modes of duty-cycle control.
- (2) Performance highly susceptible to output filter parameter changes and/or output loading (e.g., a capacitive load).
- (3) No provision to nondissipatively limit the instantaneous power-circuits. Component electrical stress during transients, such as converter starting and sudden output fault.

The Standardized Control Module (SCM), reported here in detail, mitigates all three aforementioned limitations. The improvement is realized through the design of a standardized Analog Signal Processor (ASP) and a standardized Digital Signal Processor (DSP) to process all regulator control, command, and protection signals. It is applicable to all types of converter-regulator configurations. The SCM is applied in this program to control three of the most commonly used power configurations: the buck boost, the series buck, and the parallel-inverter converters.

The standardization and the improvements are accompanied by generally superb steady-state regulation and transient responses. Output dc regulation of 0.1% is routinely accomplished under wide line, load, and temperature variations. Dynamic output regulation of less than 1% is met under a two-to-one step input voltage change, a no load to full load step, or a 10% audiosusceptibility test (i.e., 2.8V RMS superimposed on a 28V dc input, 10Hz to 10MHz).

The universal nature of the SCM hardware is matched by a generalized analysis program employing state-space techniques and providing an unified description for all switching regulators using any duty-cycle control mode.

With all these merits, this control module is expected to find its way into various high-performance military and space applications. To support this goal, a follow-on effort is presently underway to compile a SCM design handbook which, upon its completion, will enable a prospective SCM user to design readily the various SCM circuit parameters in order to meet a set of specified performance requirements. A regulator design will then become a routine task insofar as the control-dependent performances are concerned.

2. INTRODUCTION

The function of a power processor is to provide the electrical compatibility between its energy source and various loads. Except in special cases where voltage step-down is achieved through dissipative means, power processors operated from a dc source generally depend on inductive phenomena as the basis for voltage transformation. Such systems must be oscillatory in nature due to the finite flux capacity of the inductive elements, which leads to the general use of high-frequency switching to realize power processor size and weight savings. Consequently, the power processor control system must be able to accept analog signals emanating from the sensing circuit and the control reference, and convert them into discrete time intervals in controlling the conduction and nonconduction of the power switch.

The electrical performance of a power processor depends, to a large extent, on the quality of its control system. While there have been numerous control circuits proposed and in use today, most of these circuits suffer one or more of the following imperfections that tend to restrict their respective utility:

(1) Inability to Perform Different Modes of Duty-Cycle Control

Various control laws can be used to govern the power switch conduction (ON) and nonconduction (OFF) intervals to achieve a given control objective. In terms of timing implementation, the available means are the following:

- Constant on-time T_n , variable off time T_f
- Constant T_f , variable T_n
- Constant $(T_n + T_f)$, variable individual T_n and T_f
- Variable T_n , T_f , and $(T_n + T_f)$

While it is true that quite often only the achievement of the control objective is important, and that the means employed to accomplish the objective is irrelevant as long as all specifications are met, there are other power processors for which the use of a given means of duty-cycle control is necessary. For example, requirements on synchronization and electromagnetic compatibility may dictate a control based on constant $(T_n + T_f)$, whereas in

certain LC resonant applications the sinusoidal current in the power switch for one half of the LC resonant cycle inherently demands a control based on a constant T_n and a variable T_f . Consequently, a truly standardized control module for switching power processors should be capable of implementing a maximum number of duty-cycle control means through minimum circuit changes.

(2) Inability to Provide Immunity to Output-Filter Parameter Changes

Sources of output-filter parameter changes are initial component tolerances, temperature variations, aging, and most importantly, the possible reactive nature of the power-processor load. For example, it is not uncommon for a load user to have in his load package an input filter having a higher capacitance than that in the power-processor output filter. Being the last to absorb all the requirements imposed to it by the various loads it serves, a power processor seldom enjoys the luxury of having the nature of its loads well defined when it is under development. As a result, the compensation networks of most existing control circuit are devised from consideration of the power-processor output filter alone assuming a resistive load, and exotic means of pole cancellation has been the prevailing art in negating the second-order filter effect to achieve stability and well-damped responses. Needless to say, such a cancellation can miss its mark badly when tolerance, temperature, aging, and more importantly, the reactive loading, have collectively made their presences felt. Inasmuch as the output filter provides the dominant second-order corner frequency of the feedback loop critical to power-processor stability and performance, a truly standardized control module for switching power processors should be capable of providing a maximum immunity to effects of output-filter parameter changes due to tolerance, temperature, aging, and reactive loading.

(3) Inability to Provide Power-Component Stress Limiting

One of the most lagging aspects of power processing technology at present is that of reliability. The reliability of the power processors can be greatly enhanced by controlling the power component stresses during steady state and, more important, during dynamic operations such as step line and/or load changes, sudden output short circuit, and converter starting. Without this stress control, the reliability data based on the aggregation of component statistical failure rates becomes meaningless, and no amount of elaborate quality assurance can increase the level of confidence. Thus in the magnetic-semiconductor, transient-prone power processors, the means to achieve reliability enhancement

is to implement circuit techniques to limit, on an instantaneous basis, the electrical stresses in all power processor components, thus ensuring safe operation during steady state and transients. Existing power processors often forsake this limiting function, and instead rely on generous derating of all power components to foster reliable operations*. Such a practice not only places the processor to remain at the mercy of uncontrolled transient stresses, but it will become inevitably impractical in view of the future trend of higher power applications. Consequently, a truly standardized control module for switching power processors should be capable of providing power component stress limiting and working in unison with the basic regulation control to maintain orderly and predictable steady-state as well as transitional operations between steady states.

The three lagging aspects of existing control circuits in general have served to define the major objectives of a Standardized Control Module (SCM). As a forerunner of the SCM effort, contract NAS3-14392 was consummated in 1972 where a multiple-loop concept [1, 2, 3] and a common digital interface circuitry [3] were applied to control three most commonly used dc to dc power processor configurations, namely, the buck regulator, the buck-boost converter, and the parallel inverter. The present effort, under contract NAS3-18918, was performed between July 1974 and October 1975 to provide continued improvements in all three aforementioned areas, which has produced the following program highlights:

- A digital signal processor design of enhanced commonality capable of implementing different duty-cycle control means through different interconnections of component terminals.
- The generation of a discrete-time control-loop model suitable for (A) analyzing power processors operating with either a continuous or a discontinuous output-filter inductor current, and (B) performing cost-effective simulation. The analysis identifies the optimum design for filter immunity.
- The achievement of coherent compatibility between the basic regulation control circuit and the stress-limiting circuit for all duty-cycle control means under all operating conditions.

* Some converters have been equipped with an average current limiting function, i.e., with a current regulator. However, the time response of such a regulator is usually so slow that it serves no function insofar as instantaneous stress limiting during a transient condition is concerned.

These three accomplishments have greatly enhanced the goal of improvising a power-processor control circuit intended for use as a Standardized Control Module (SCM).

Detailed information concerning the SCM effort of this program phase will be presented in Sections 3 to 8. Starting with the presentation of a SCM functional block diagram in Section 3, the Standardized Analog Signal Processor of the SCM are given in Section 4. Provided in Section 5 is the Digital Signal Processor. Detailed SCM circuit descriptions and breadboard test results are given in Section 6. The SCM modeling and analysis results are shown in Section 7. Major conclusions of the program are then summarized in Section 8. A number of technical details are reserved for presentation in Section 9, Appendices.

3. STANDARDIZED CONTROL MODULE FUNCTIONAL BLOCK DIAGRAM

Functionally, a power processor can be divided into two parts: the power circuit and the control circuit. By definition, the power circuit handles the energy transfer from the source to the load. Minor modifications are many, but there are only three basic types of power circuits: the buck, the boost, and the buck-boost. These circuits have been thoroughly described in literature [4,5], and the familiarity of these circuits on the part of the readers is assumed.

As a function of the load demand, the rate of the source-load energy transfer is managed by the control circuit through a set of prescribed control objectives. During nominal steady-state and transient operations, the objectives are normally associated with (A) The tracking of a certain output quantity in accordance with a given control reference signal, and (B) The compliance of all other power-processor performance specifications such as source EMI, output ripple, audiosusceptibility, output impedance, etc. During abnormal operations involving out-of-nominal line and load conditions, the objective becomes the control of power-component electrical stresses to provide effective protection against (A) catastrophic/degradation component failures within the power processor, (B) the voltage collapse of a current-limited power source feeding the processor, and (C) the possible damage of load equipment powered by the processor. A control circuit thus serves the dual functions of regulation and protection, which become the overriding concern of the standardized control module (SCM).

The goal of this section is to present a SCM block diagram, through which the detailed functions performed by the SCM can be described. The presentation starts with a functional block diagram for conventional single-loop power-processor control circuits. The functional handicaps revealed by such a block diagram are reviewed, and the subtle differences between the conventional control and the specific SCM used in this program are evolved. The section ends with a SCM functional block diagram and its descriptions.

3.1 FUNCTIONAL BLOCK DIAGRAM OF A CONVENTIONAL SINGLE-LOOP POWER PROCESSOR

Before describing the details of signal processing within a single-loop controlled switching regulator, it is worthwhile to provide a generalized view on the analog-signal-to-discrete-pulse conversion process. To begin with, the analog signal at the output of the power processor can be utilized in two different ways:

- (1) The instantaneous information of the analog signal is utilized directly to formulate the discrete-pulse time interval. This mode of operation has been frequently referred to as the "free-running" type; there is no externally-generated timing reference to restrain the duration of individual on- or off-time pulse interval. [6, 7, 8, 9]
- (2) The instantaneous information of the analog signal is not used in formulating the discrete-time interval. Instead, the average information of the analog signal is utilized in conjunction with a variety of timing mechanisms to achieve various duty-cycle control. The timing mechanism may produce either a constant T_n , a constant T_f , a constant $(T_n + T_f)$ with variable T_n and T_f , or a variable $(T_n + T_f)$ with T_n and T_f also variable. In each case the average information of the analog signal is processed to produce a time interval complementary to the established timing constraint in order to fulfill the control objective. [10, 11, 12, 13]

Common to both methods of analog-signal utilization is the need for a ramp function to intersect a threshold level to define the initiation or the ending of a pulse duration. When the instantaneous information of the analog signal is utilized directly for pulse formulation, the instantaneous waveform of the analog signal itself containing an ac component provides the necessary ramp function, and two threshold levels, one upper and one lower, are needed to define the on- and off-time intervals to complete a switching cycle. On the other hand, when the average information of the analog signal is used in unison with a given timing reference, such as constant T_n or constant $(T_n + T_f)$, the intersection of the ramp function with only one threshold level is needed to define an operating cycle by controlling the complementary timing interval that is not constrained

by the timing reference. In this case, only a single threshold level is necessary; the implementation of more-than-one threshold level is neither needed nor wanted.

The discrete pulses thus formed become the output of the control circuit. This output is applied to control the operation of the power circuit; the power circuit then converts the discrete pulses back to an analog signal, which is in turn sensed by the control circuit in a closed-loop fashion. Consequently, a conventional single-loop power processor can be divided into three distinct conversions:

- (1) Discrete-time-pulse-to-analog-signal conversion in power circuit
- (2) Analog-to-analog signal conversion for ramp forming
- (3) Analog-to-discrete-time conversion via ramp-threshold intersection

Using the functional block diagram shown in Figure 1, these three conversion processes are further described as the following:

3.1.1 Discrete-Time-Pulse-to-Analog-Signal Conversion

The conversion takes place within the power circuit of a power processor. The power circuit, occupying the upper division of Figure 1, is composed of the basic power stage and the power switch drive. The basic power stage contains the input filter, the power switches, and the output filter. The power-switch drive serves to interface between the control circuit and the power stage. Faithfully transmitting to the power-switch the discrete-time intervals derived from the control circuit, the power-switch drive also provides (A) impedance matching between power and control circuits, and (B) speed-up turn-off of the power switch at the end of a discrete on-time interval. Voltage or current pulses thus formed within the power stage are then averaged by an output filter, which generally has a much longer time constant than the discrete-pulse intervals. The averaged output thus contains only a small percentage of ac component superimposed on a dc value.

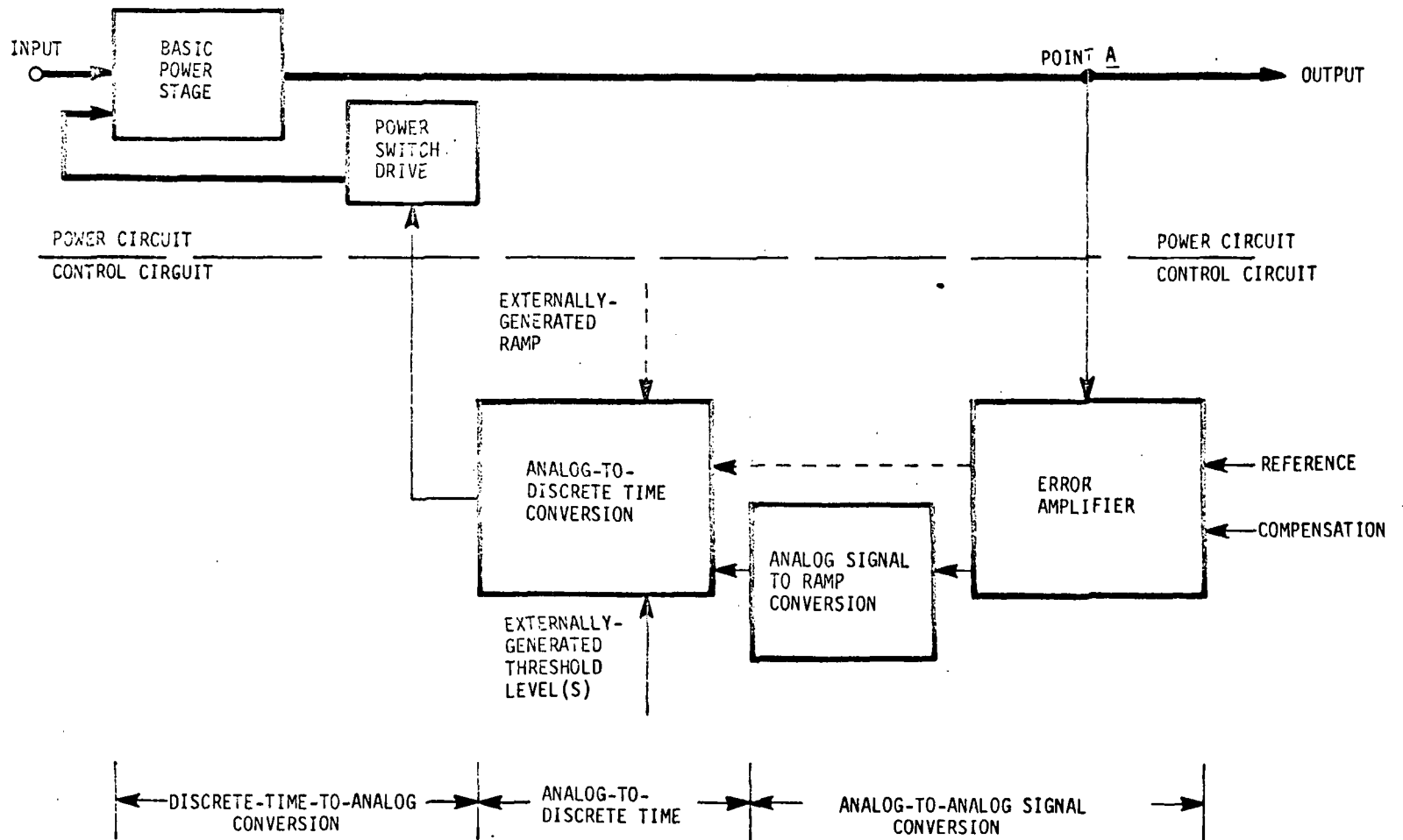


FIGURE 1 A GENERALIZED BLOCK DIAGRAM OF SINGLE-LOOP CONTROLLED CONVERTERS

The tracking of this value, shown as the power-circuit output at point A of Figure 1, to an established reference, becomes the primary control objective of the power processor. The signal is applied as the input to the control circuit to initiate the needed signal conversion.

3.1.2 Analog-to-Analog-Signal Conversion

Within the Error Amplifier block of Figure 1, the analog signal at Point A is compared with a control reference, and the error is further processed. Corresponding to the two different analog-signal utilizations described in Section 3.1, the functions performed by the error amplifier are as follows:

- (1) In the "free-running" type of control, the error amplifier is essentially a divider (a no-greater-than-unity-gain amplifier) attenuating both dc and ac components of the analog signal at point A to a level compatible with the reference. No compensation function is normally involved. The attenuated ac component at the amplifier output serves as the ramp function. The upper and lower threshold levels needed to intersect the ramp function for pulse-duration control is described later in Section 3.1.3.
- (2) In the "time-constraint" type of control, the error amplifier is essentially a properly-compensated high-gain amplifier. The nature of the amplified error is such that it generally does not lend itself for serving as a ramp function. For this error to become a useful control signal, either one of the two independent approaches represented in Figure 1 is possible:
 - (A) The amplifier output of negligible ac component is used directly as the threshold level to participate in the control of the pulse duration. [14, 15] A complementary ramp function of predetermined slope, to be discussed in Section 3.1.3, is externally generated. This implementation is shown in Figure 1 in dotted lines.

- (B) The amplifier output is transformed into a ramp through an integration process before participating in the control of the pulse duration. The transformed ramp can be a voltage ramp, which is easily obtained by applying the amplifier output to a RC circuit for periodic charging and discharging. In this case, an externally generated threshold voltage level is needed to complement the transformed ramp to effect the pulse-duration control. It can also be a flux ramp, realized by applying the amplifier output to a saturable magnetic core to effect a controlled rate of flux change. The corresponding threshold in case of a flux ramp is generally the saturation flux of the timing core employed[16]. This is shown in Figure 1 in solid lines.

3.1.3 Analog-to-Discrete-Time Conversion

This is the conversion process within which the threshold level meets the ramp function to define a pulse duration:

- (1) In the "free-running" type of control where there is no external timing constraint, the ramp-threshold intersections are needed to determine both on- and off-time intervals. The intersections must define the initiation of on time, the termination of on time, the initiation of off time, and the termination of off time. However, the termination of one interval generally coincides with the initiation of the other. Thus, within a given cycle starting at the intersection initiating the on-time interval, only two more intersections defining the end of on time (i.e., the initiation of off time) and the end of off time are needed. To provide the required intersections, the simplest ingredients are dual threshold levels and ramp functions with contrasting slopes (i.e., ascending versus descending). In free-running power processors, the ramps are directly provided by the ac component of the analog signal divided down from point A of Figure 1 by the error amplifier. Dual threshold levels are generally obtained through a bistable hysteretic trigger configuration [17].

- (2A) In the "time-constraint" control where the amplifier output is used directly as a threshold level that varies as a function of the error sensed at point A, the threshold level is complemented by an externally-generated ramp function. The ramp function in most cases is of fixed slope, although in certain applications a variable slope varying proportional to the power-processor input voltage has been implemented for its apparent "line compensation" advantage [18]. Regardless whether the slope is fixed or not, the ramp-threshold combination is only effective during one timing interval in the "time-constraint" type of control. If the time constraint predetermines the on time (off time) interval, the ramp is effective during the off time (on time). If the time constraint applies to a constant sum of on-time and off-time (i.e., a constant-frequency operation), then the ramp can be effective during either the on-time or the off-time, but not both.
- (2B) In the "time-constraint" control where the amplifier output is integrated to form a ramp, it is complemented by an externally-generated threshold level. While the ramp slope may vary as a function of the sensed error at point A, the threshold level is generally fixed, although in few applications a variable level has been implemented in an attempt to achieve a faster power-processor response [19]. Similar to (2A), the ramp-threshold combination is effective only during either the on time or the off time, but never both.

The discrete intervals formed through the process described in either (1), (2), or (2B) are then applied to control the power stage of Figure 1 through the power-switch drive described in Section 3.1.1, thus completing the signal path within a conventional single-loop controlled power processor.

3.2 FUNCTIONAL HANDICAPS OF A CONVENTIONAL SINGLE LOOP POWER PROCESSOR

Discussed in the following sections are the imperfections restricting the utilities of numerous existing single-loop control circuits in terms of performing different duty-cycle control modes, power-processor steady-state and transient performances, and power processor component stress limiting. As presented in Section 3.1, two major categories of existing single-loop power-processor control are the "free-running" type and the "time-constraint" type. Based on imperfections associated with each type, the desirable features of a Standardized Control Module (SCM) can then be identified and realized through improved control-circuit implementation.

3.2.1 Handicaps in Performing Various Duty Cycle Control Modes on AT Switching Regulators

A competitive SCM must accomplish the following:

- Capable of performing a maximum number of duty-cycle control modes including constant on time and constant frequency.
- Adaptable to all switching regulator types.
- Applicable to either a continuous or discontinuous output filter inductor current, i.e., either without or with a zero-current dwell time.

In relation to these requirements, existing free-running and time-constraint types of control are assessed as the following:

(1) Free-Running Control

- The power processor is characterized by the heavy dependence of its switching frequency on the amount of equivalent series resistance (ESR) in the output-filter capacitor. For a given ESR, the essentially fixed ramp slope during the off time of the power switch tends to work in unison with a fixed hysteretic width (between the dual threshold levels) to produce a constant off-time duty-cycle control in steady-state operation. It is therefore unable to engage in constant on-time or constant-frequency control.*

*Recent development of variable hysteresis width has made constant-frequency operation possible in a multiple-control-loop implementation. [20]

- The ramp slope at Point A of Figure 1 must have contrasting slopes during on time and off time. This condition holds in the buck regulator when the effect of ESR in shaping the ramp is significant; it no longer holds in the buck boost or boost regulator with similar ESR effects. Since the ESR is generally a more dominant ripple-producing element than the capacitance charge and discharge, the control so far has been limited to buck regulator and its equivalent. [6, 7, 8].
- Applying free-running control to discontinuous-current operation is difficult for similar reasons stated above. The relatively flat portion of the ramp function during the zero-current dwell time and its closeness to the lower threshold level makes noise-free repetitive switching difficult to achieve.

(2) Time-Constraint Control

- With the external time constraint selected by the designer, the control is capable of implementing any duty-cycle mode. Reliance on the power-processor output average information rather than its instantaneous ripple for error sensing also removes all restrictions regarding the applicability to different switching-regulator power circuits operating in either continuous or discontinuous output-inductor current.
- The ramp or the threshold level depends on amplified error at the amplifier output over the entire controllable time interval, during which an external complementary threshold or ramp is generated. The concurrent internal/external threshold-ramp formations must be accomplished by specific circuits. Different control and protection philosophy imbedded in various duty-cycle control modes generally requires quite different circuit implementations to realize the desired functions. It is thus difficult to achieve different duty-cycle controls based on different inter-connections within a common control-circuit configuration.

3.2.2 Handicaps in Power Processor Performances

Desirable performance features of a SCM include the following:

- High degree of immunity to noises attendant to fast and high-current switching
- Minimum variation of power-processor performance as a function of component parameter changes due to tolerances, environments, aging, and external loading. The performance characteristics most commonly identified with the control circuits are stability, regulation, and line and load sinusoidal/step transient responses.

In relation to these requirements, existing free-running and time-constraint types of control are assessed as the following:

(1) Free-Running Control

- In this type of control, the switching spikes attendant to high-current switching can intersect the threshold level, and deprive the legitimate ramp function of its role in dictating the on-off of the power switch. For example, using free-running control for a preregulator and coupling the preregulator output to a dc-to-dc parallel-inverter converter (such as a Royer circuit or a Jensen circuit) may result in the preregulator switching frequency being sunk to that of the parallel inverter. Such a "noise synchronization" may cause havoc in the system if the designs of the preregulator and the dc-dc converter are independently conceived (e.g., by two vendors) to operate at drastically-different frequencies.
- The excellent stability and dynamic responses of power processors using single-loop free-running control have been well established. However, the dc output voltage is a function of the instantaneous output ripple waveform; its average value within the boundary of two hysteretics is not precisely controlled for a single-loop regulator.

(2) Time-Constraint Control

- Since the average information is now used to determine a time duration complementary to a constrained time interval, the switching spikes and other switching-related noises no longer directly effect the on-off of the power switch. While these noises may still assert themselves indirectly through a weak control-circuit component of low noise immunity, (e.g., a TTL gate) generally they can be negated through proper packaging techniques.
- Due to the presence of a second-order low-frequency energy-storage element and the lack of dual threshold levels to constrain the output response, the utilization of a high-gain and wide-bandwidth amplifier for good static and dynamic regulation usually results in an increasing risk of instability. While the stability can be enhanced through various second-order pole-zero cancellation techniques, the cancellation becomes grossly ineffective in the face of cumulative component changes due to tolerances, environments, aging, and most importantly, external loading; the last factor is generally unknown in the power-processor development stage.

3.2.3 Handicaps in Power-Processor Power Component Peak Stress Control

The need for peak-stress control is promoted by the fact that one of the most lagging aspects of power processing to date is that of reliability. By this is meant the failure to consistently achieve in operational equipment the reliability that one might anticipate from consideration of the reliability of components themselves. Most equipment failures occur during line or load transients when the peak stress in the failed component exceeds its safe operation region, which justifies the need for peak-stress control. Furthermore, a significant number of present and future loads, such as the traveling wave tube, the ion engine, and the laser application, are hostile in nature as they encounter arcing either regularly or on an off-nominal basis. Needless to say, power processors for such loads must be peak-stress protected; the existing average-stress type of current limiting is simply too slow to reliably control the peak dissipation in all vulnerable components for these types of power processors.

Existing power processor control circuits often forsake the peak-stress control. As mentioned in Section 2, this practice is not only risky, but becomes impractical in view of the forthcoming higher power trend.

Regardless the free-running or the time-constraint type, the present lack of component peak-stress control in existing power processors is due mostly to ignorance of the need, rather than any difficulty in its implementation. Consequently, the handicap described in this paragraph should not be regarded as inherent to existing single-loop power-processor control circuits. Rather, it serves as a reminder that the provision of power component peak-stress control must be an integral part of an improved SCM.

3.3 SUMMARY OF NEEDED IMPROVEMENTS FOR SCM

From the foregoing discussion, the improvements needed for a SCM are identified as follows:

(1) Inherent Ramp Formation:

A major difficulty to enable various duty-cycle control modes within a common control-circuit configuration (through different interconnections) has been the different functional requirements of internal/external ramp-threshold formations associated with each type of duty-cycle control. This difficulty can be minimized if the ramp formation during on- and/or off-time can be derived from inherent switching waveforms within the regulator power circuit. Elimination of the circuit needed for external-ramp generation or internal analog-signal-to-ramp conversion will serve to release significantly the circuit complexity, thus enhancing the possibility of designing a SCM capable of various duty-cycle control modes and applicable to all switching regulator types operating with continuous or discontinuous output-inductor current.

(2) Autocompensation of Second-Order Filter

With the existing pole-zero cancellation ineffective against component and loading changes, compensation of the low-frequency second-order filter should ideally be achieved adaptively, i.e., any output-filter component parameter change is met with a corresponding change in the compensation network such that an effective pole-zero cancellation is maintained automatically independent of filter parameters. Intuitively, such an achievement must involve the sensing and processing of inductor voltage or capacitor current associated with the output filter. No adaptive compensation of the second-order filter is conceivable without utilizing its state variables for control purposes.

(3) Peak-Stress Limiting

Two important points to be observed in peak-stress limiting are:

- (1) The implementation should be simple and its benefits wide-spread to cover a maximum number of power components, (2) the implementation should allow both steady and transient peak-stress limiting actions without causing attendant problems such as incomplete reset of magnetics or incompatible operation between the basic control circuit and the stress-limiting circuits for all power-circuit types under various duty-cycle control modes.

These improvements are designed into the SCM. The SCM functional block diagram is presented next.

3.4 FUNCTIONAL BLOCK DIAGRAM OF A MULTI-LOOP SCM-CONTROLLED POWER PROCESSOR

A SCM-controlled power processor block diagram is shown in Figure 2. The power circuit shown in the upper half of Figure 2 is identical to that of Figure 1. The control circuit, now labelled SCM, is shown in the lower half of Figure 2.

In terms of signal processing, the power processor of Figure 2 can be separated into four major portions:

- (1) Discrete-time-pulse-to-analog-signal conversion
- (2) Analog-to-analog-signal conversion
- (3) Analog-to-digital-signal conversion
- (4) Digital-to-discrete-time-pulse conversion

These four conversion processes are described in the following sections.

This block diagram will lead to detailed discussions on the theory and practice of the SCM-topics of the subsequent sections.

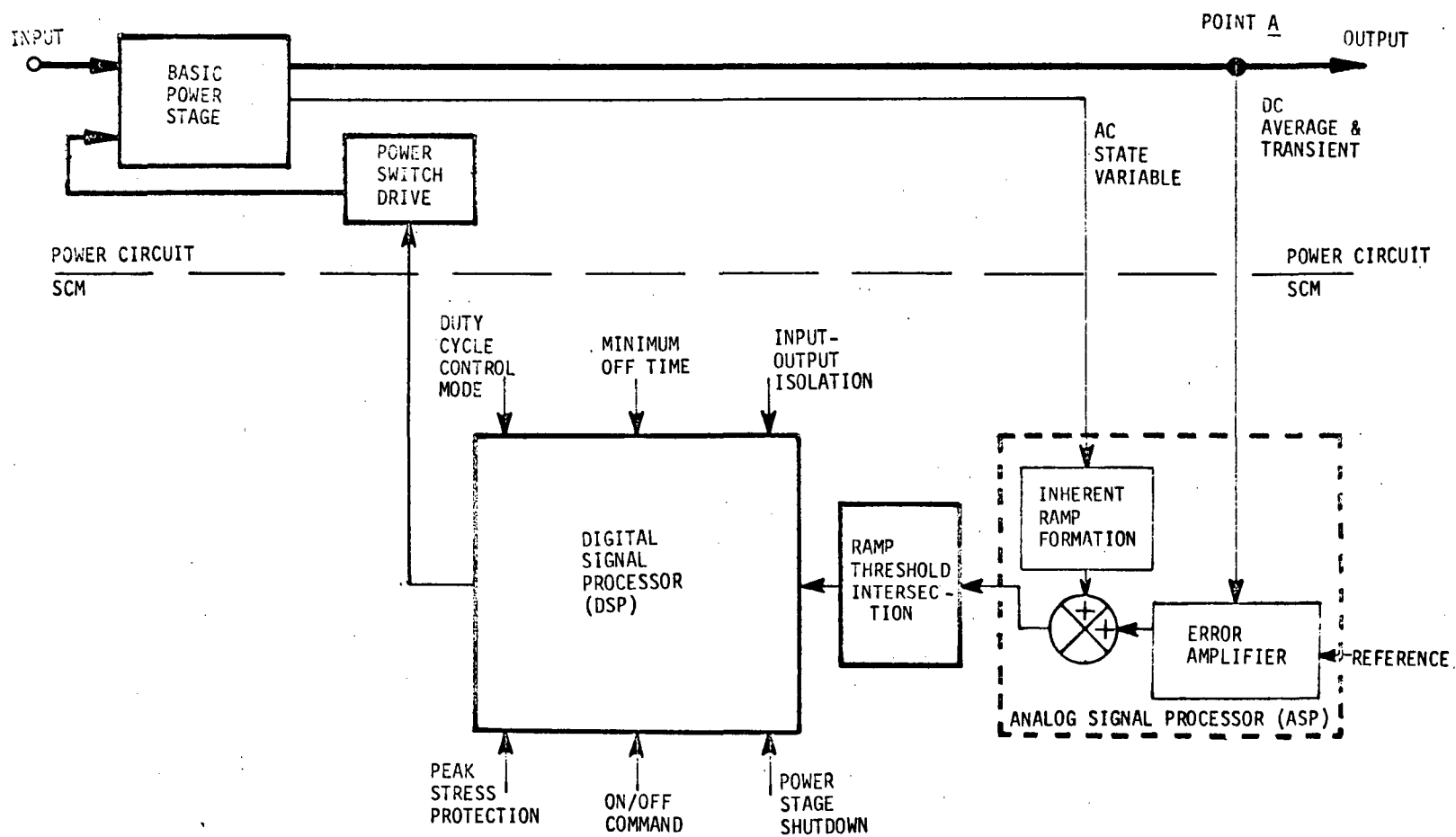


FIGURE 2 BLOCK DIAGRAM OF SCM-CONTROLLED MULTIPLE-LOOP CONVERTERS

3.4.1 Discrete-Time-Pulse-to-Analog-Signal Conversion

The discrete-time pulses generated from the control circuit of Figure 2 is applied to the power-switch drive, causing a voltage or current pulse train to occur within the power stage. Similar to the single-loop control of Figure 1, the power-stage output at point A of Figure 2 represents the dc average information of the pulse train, i.e., an analog signal.

3.4.2 Analog-to-Analog-Signal Conversion

While in Figure 1 the signal at point A is the only analog signal resulting directly from pulse train and serving as the input to the error amplifier, in Figure 2 the discrete-time pulse is further used in conjunction with the power stage for the purpose of providing the inherent ramp formation outlined in Section 3.3. The error processor and the inherent ramp formation are combined to form an Analog Signal Processor (ASP) shown in Figure 2. Similar to Figure 1, the signal sensed at point A is compared with a reference, and the error is amplified to appear at the ASP output.

In addition, an ac signal within the power stage is used as an additional input for inherent ramp generation. The ramp may be obtained by integrating the rectangular ac voltage pulses across the output-filter inductor, or by directly utilizing the ac current in the output-filter capacitor. The sum of dc and ac signal processing becomes the output of the analog signal at the ASP output. Other than the ramp formation, the significance of the ac loop in terms of control-loop stability will be addressed in a later section. For the time being, it suffices to state that the SCM autocompensation of output-filter and loading changes is a direct result of this added ac loop.

The fact that the ramp formation is originated from a state variable inherent within the power-stage energy-storage elements enhances the universality of the SCM; these state variables are always present in all switching regulators operating in continuous/discontinuous filter inductor current and in all duty-cycle control modes. Furthermore, the elimination of the extra ramp generator reduces considerably the circuit complexity, thus promoting the ease of physically implementing the SCM concept.

3.4.3 Analog-to-Digital-Signal Conversion

The function of this block is to intersect the ASP analog output, which contains the amplified dc error and the ramp, with an externally-generated threshold level. A digital signal is issued at the output of this block when the intersection occurs, which serves to initiate a switching event for the power switch. Once the switching event is initiated, its duration is determined by the Digital Signal Processor (DSP) to be discussed in the next section.

Consequently, the function of this block is to interface between the ASP and the DSP, with the intent of releasing the ASP of any influence in prescribing the duty-cycle control mode. Unlike the error amplifier output of the single-loop control shown in Figure 1, the ASP output of Figure 2 is neither used as a threshold level nor integrated into a ramp. A SCM user is thus free to select the desirable duty-cycle control mode from all possible choices implemented in the DSP, thereby achieving a greater degree of flexibility.

3.4.4 Digital-to-Discrete-Time-Pulse Conversion

This conversion block, labelled Digital Signal Processor (DSP) in Figure 2, can be regarded as the nerve center of the control system, as it must process all incoming signals and transmit the correct output signal to operate the power switch. The signals processed by the DSP can be divided into two categories: control and protection/command.

(1) Control Signals Processed by DSP

- Regulator Control:

The regulator control signal is the digital signal derived from the output of the aforescribed analog-to-digital-signal conversion block. Upon receiving the signal, the DSP will proceed to issue a discrete-time pulse to prescribe the on time or the off time of the power switch.

- Duty-Cycle Control:

This control signal determines whether the duty cycle of the power switch is to be constrained by constant on-time, constant off-time, constant frequency, external synchronization, or other possible modes.

- Minimum-Off-Time Control

This signal prescribes the minimum nonconduction time intervals of the power switch following the termination of each conduction interval due to regulator control or peak-stress protection. Such nonconduction intervals are needed to allow complete flux reset of the main energy-storage inductor and the power-switch base-drive magnetics during transient operations such as converter starting and load arcing.

- Input/Output Isolation

The function here is to satisfy frequent applications requiring source/load to be isolated by a large impedance (greater than $10M\Omega$).

(2) Protection/Command Signals Processed by DSP

- Peak Stress Protection

The signal is used to control the peak electrical stresses of major power-handling components. Over the normal steady-state operation, there is no peak stress protection signal. However, it appears at the instant when a transient power-switch current greater than a pre-set value is detected. The signal is processed by the DSP to effect an immediate turn-off of the power switch (subsequent to the elapse of the power-switch storage time, of course). Following a controlled off time, the power switch is turned on again. If the cause for the excessive peak current is no longer present, the peak-stress protection signal will again disappear. If the cause persists, so will the signal. Consequently, the protection essentially limits the power-switch current to a pre-set value during any line or load transient including converter starting and output fault.

The reason to choose the power-switch current for peak limiting is that in any type of power processor the switch is invariably placed in series with the main power magnetics during the conduction time. By virtue of the facts that the MMF of the power magnetics cannot change instantaneously, and that the electrical stresses on all power components including those of input filters, output diodes, and output filters are intimately related to the instantaneous MMF in the power magnetics, the peak-stress protection essentially controls the stresses of all power components during all operating conditions. This is the approach through which the SCM achieves the intended peak-stress control for reliability enhancement.

- Power Stage Shutdown

The signal is generated upon a long-duration input-source undervoltage or output-load overvoltage/overcurrent, which generally are manifestations of persistent line/load abnormality or circuit malfunction. In these cases, a signal will be provided to shutdown the power stage when the faulty duration exceeds a pre-set time interval, thus protecting the source and/or the load. Only an external command can restart the power processor, which will shutdown again if the faulty cause persists.

- On-Off Command

The signal is externally applied to enable command on-off of the power processor.

The foregoing discussions have provided a general overview of existing single-loop control circuits and their limitations, from which the improved concept of SCM is introduced. The unique system, including the ASP, the DSP, and their combined operation in controlling a power processor, will be presented in detail in the following sections.

4. THEORY AND PRACTICE OF ANALOG SIGNAL PROCESSOR (ASP)

As stated previously, the ramp derived from the Analog Signal Processor (ASP) is based on state variables within the output filter. This method of ramp formation not only simplifies the design complexity and promotes circuit commonality of various duty-cycle control, it also achieves (1) adaptive autocompensation of the output-filter parameter changes, and (2) instantaneous duty-cycle adjustment capability.

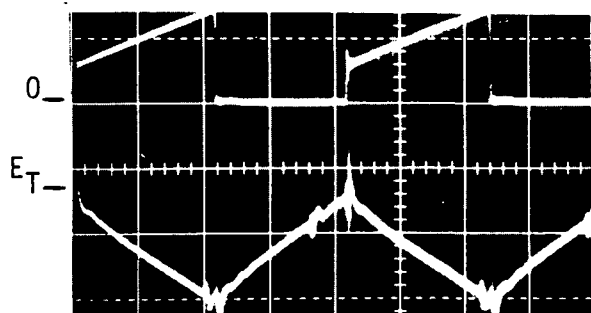
Within this section, the ASP-related design details and performance features are presented. Starting with the basic ASP circuits, the discussion will be followed by proper choice of state variables for ramp generation. SCM features of autocompensation and instantaneous duty-cycle adjustment are described. The ramp-threshold implementation of the SCM as a function of the given duty-cycle control mode, along with a certain SCM operation subtlety involving constant-frequency control, are then clarified.

4.1 BASIC ASP CIRCUIT CONFIGURATION

The ASP configuration is represented in Figure 3 using a switching regulator for illustration. The error processing component is a high-gain amplifier. Three input signals are applied to the amplifier through three feedback loops working in unison.

The first loop senses the dc output e_o at point A, divides it by a factor K_d , and compares to amplifier reference E_R . The difference $e_{dc} = K_d e_o - E_R$ becomes the dc error. In conjunction with externally-generated threshold level E_T , the dc output of the amplifier is determined by e_{dc} . The loop therefore corresponds to the error amplifier block of both Figure 1 and Figure 2. It is no different than any of the single-loop error amplifier.

The second loop senses the state variables associated with the output filter for ramp formation. The variable can be the ac voltage ($e_i - e_o$) across the filter inductor, or the ac current i_c in the filter capacitor. For dc-to-dc converters in which the ac filter inductor voltage is of rectangular waveform, a triangular ramp is conveniently achieved through the integration of the rectangular voltage. In this case the amplifier is configured with a capacitor feedback to serve a dual function of amplification



25

and integration. On the other hand, when filter-capacitor current is used for ramp generation, the integration process may or may not be necessary. For the buck switching regulator shown in Figure 3, the triangular capacitor current (during continuous-output-filter-inductor-current operation) becomes a legitimate ramp by itself; it can be directly utilized as the ramp. Conversely, for a continuous-current buck boost converter with trapezoidal capacitor current, the utilization of such a waveform as the basis of the ramp is impossible without further integration. The choice of a proper state variable for ramp formation is further elaborated in Section 4.2.

The third loop shown in Figure 3 consists of either a capacitor or a capacitor-resistor network, connecting from the output of the output filter to the sensing input of the error amplifier. Its function is to sense any change in de_o/dt , and feed the change to the integrator amplifier accordingly to improve the output transient response of the power processor. The significance of this network to transient-response improvement is described later in Section 4.4.2.

4.2 CHOICE OF PROPER STATE VARIABLE FOR RAMP GENERATION

The state variable chosen for ramp generation must satisfy the following criteria:

- (1) It is an inherent ac waveform so that it will not affect the input and output dc balance of the average-sensing error amplifier.
- (2) Its waveform is either a directly-utilizable ramp or easily processed to produce a ramp. While the ramp is not required to exhibit linear slopes during on time and/or off time, preferably it will have distinct peaks and valleys that correspond to the initiation of on- and off-time intervals of the power switch. Such correspondences tend to ease the complexity of the SCM control-circuit implementation.
- (3) It must provide the intended autocompensation of the output-filter parameter change.

The first criterion restricts the choice to either the voltage across the output-filter inductor or the current in the capacitor, as they are the only two steady-state waveforms that are inherently ac.

Regarding the second criterion, the adaptability of these two waveforms depends on the power processor power-circuit configuration. When the inductor voltage is integrated to produce a ramp, the second criterion is satisfied for the buck, the boost, and the buck-boost power processor. The universality is made possible by the fact that the inductor-voltage waveforms for all three configurations are rectangular; the integration of these voltages invariably produces triangular waveforms whose peaks and valleys initiate the controlled on- and off-time intervals. On the other hand, the same universality is not enjoyed by the capacitor current. The buck-regulator output capacitor current is inherently triangular, allowing such a waveform to be transported to the ASP output and used directly as the ramp. The direct utilization, however, does not apply to either the boost or buck-boost configuration. The waveform of the capacitor current in these configurations is trapezoidal. Additional integration is necessary before a ramp function can be derived.

The assessment of the third criterion depends on results of qualitative control-loop design-oriented analysis, which is presented in Section 4.3. It suffices to say at this time that the autocompensation of the output-filter parameter change is achievable when the integration of the inductor voltage is used as the ramp-producing mechanism.

Consequently, based on consideration of universal adaptability and filter autocompensation, the output-filter inductor voltage is selected as the basis for ramp formation.

4.3 SCM FEATURE OF OUTPUT-FILTER AUTOCOMPENSATION

An observable feature of the SCM is its capability of output-filter autocompensation, i.e., in a properly-designed SCM the regulator stability can be made quite immune to the change of output filter inductance and capacitance. As previously stated, this feature releases the designer of the frequent concern on the effect of filter parameter change due to component tolerance, temperature, aging, and more importantly, due to the effect of regulator loading; the nature of the load is often unknown to the designer at the time when the regulator is being designed.

Frequency-domain stability representation through Bode Plot of the open-loop transfer function was performed to provide the analytical insight into this feature. Details of the analysis are reserved for presentation in Section 7, SCM Modeling and Analysis. For the time being, it suffices to point out several key findings:

- (1) In assessing the stability of a multiple-loop system such as a SCM-controlled switching regulator through its open-loop transfer function, the location at which the analyst chooses to mentally "open" the loop is of utmost importance. Opening the loop at different locations within different loops of a multiple-loop system generally calls for different interpretation of the analytical results.
- (2) The correct place to open the loop in order to assess SCM regulator stability through its open-loop transfer function is at the output of the integrator amplifier.

- (3) As stated previously in Section 4.1, there are three feed-back loops in the ASP; the dc loop, the ac loop, and the transient loop. A design criterion for the first two loops is identified through analysis, with which ideal autocompensation of the output-filter parameters, and therefore the optimum regulator stability, can be achieved without the third loop.
- (4) The function of the third loop is to improve the transient response, i.e., to change the damped oscillation into a critically-damped appearance. In doing so it actually detracts the first two loops from achieving the ideal autocompensation. This SCM trait differs significantly from a single-loop control in which a change from damped oscillator pattern to a critically-damped one invariably signifies an improvement in stability margin. This is not necessarily so in a multiple-loop system such as a SCM-controlled regulator. In fact, such an output-response pattern change may be actually accompanied by a degradation of stability margin in the SCM regulator.
- (5) If the design criterion for ideal compensation mentioned in item (3) is not observed, the regulator may become unstable without the third loop. Stable operation may be achieved with the proper design of the third-loop compensation. However, without utilizing the basic SCM autocompensation feature, such a design requiring custom-made compensation reduces the SCM to any other conventional single-loop control insofar as the control-loop stability is concerned.

The aforementioned autocompensation design criterion, along with other analytical details, will be presented later in Section 7.1, SCM-Controlled Regulator Frequency Domain Stability Analysis.

4.4 INSTANTANEOUS DUTY-CYCLE ADJUSTMENT

As previously stated, in most control systems, either the ramp function or the threshold level is transformed from the error-amplifier output. Since the error amplifier generally derives its input from the output of the output filter, the analog-to-discrete time formation, i.e., the rate of duty cycle adjustment, is limited by the low-frequency nature of the output filter.

In SCM, however, the ramp does not depend on the error-amplifier output, and is derived from the integration of an instantaneous voltage or current waveform that is inherent within the output filter. Therefore, the control system will achieve within half of a switching cycle the correct on/off time ratio in response to a line change. Using a constant- T_{on} buck switching regulator for illustration, the manner with which this instantaneous duty-cycle adjustment is accomplished is described in Figure 4.

4.4.1 Accomplishment of Instantaneous Duty Cycle Control

In Figure 4, a given input voltage E_i is assumed. The voltage E_L across the inductor corresponds approximately to $(E_i - E_o)$ during on time T_n and to E_o during off time T_f . The mechanization is such during T_n the integrator output ramp exhibits a negative slope, while during T_f the ramp slope is positive. Every instant when the positive-going ramp intersects the threshold-detector level E_T , the threshold detector releases a pulse, which in turn generates a constant-on-time pulse through the digital signal processor DSP to cause transistor Q to conduct for a constant interval T_n . In steady-state operations, the descending ramp amplitude during T_n is equal to the ascending ramp amplitude during T_f .

At $t = T_1$, a step increase is assumed for the input voltage E_i . This increase, coupled with the negligible change in E_o at the filter output due to the long filter time constant, is instantly reflected as a voltage increase in E_L across the inductor. The sudden increase in E_L due to the step change in E_i causes instantly a steeper negative slope starting at $t = T_1$. Consequently, at the end of the fixed on-time interval, the negative ramp is terminated at a lower voltage level with respect to that prior to any increase in E_i . Starting with this lower voltage, coupled with the essentially-unchanged positive ramp slope (due to a relatively

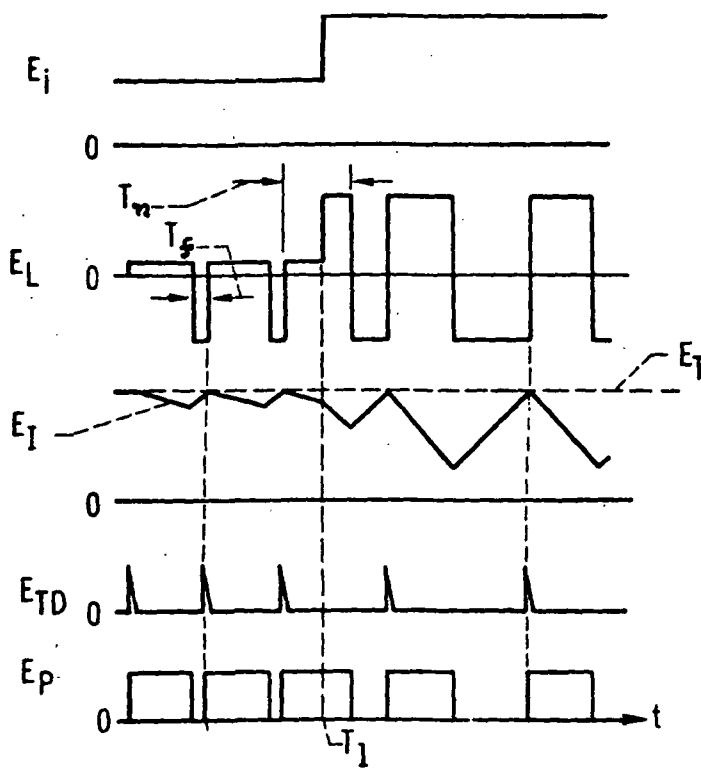
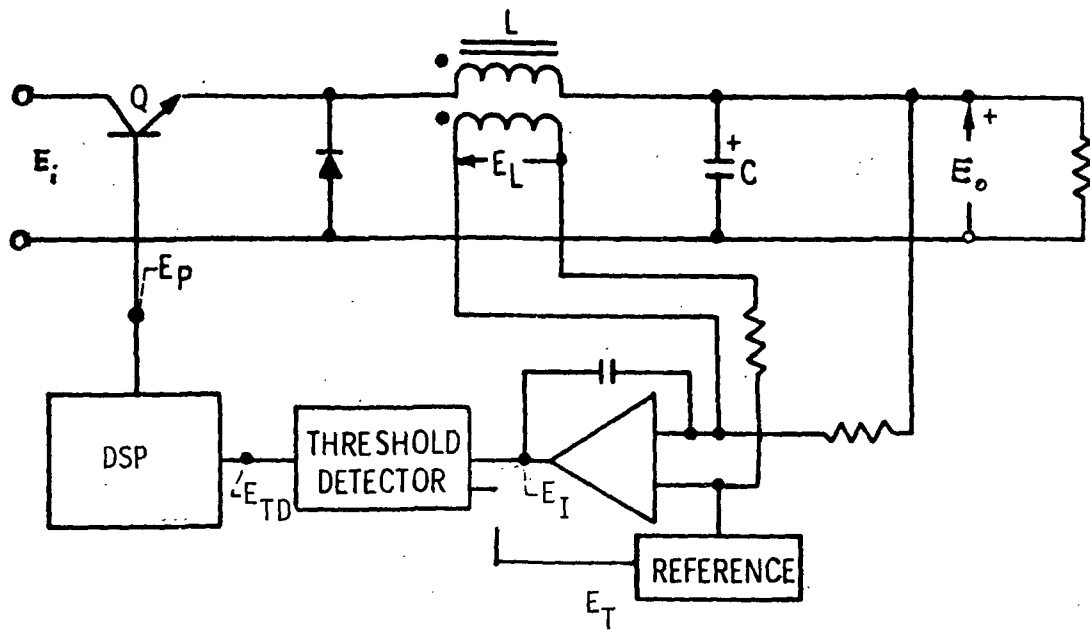


FIGURE 4 INSTANTANEOUS DUTY CYCLE ADJUSTMENT OF THE SCM

constant E_0), the immediate consequence is that it will now take a longer time before the positive ramp can again reach the threshold level. Thus, an increase of E_i under the constraint of a constant T_n is automatically met by an elongation of T_f , within the very operative cycle when the step increase in E_i occurs. Subsequent to the initial adjustment, the T_n/T_f ratio of succeeding cycles inherently maintain their correct operating values, as is shown in Figure 4.

While the description is based on a buck switching regulator with the constant- T_n control, it is easily extended to any other converter configurations using different duty-cycle control modes. The instantaneous duty-cycle adjustment is therefore a SCM property that is inherent and universal.

4.4.2 The Effect of Instantaneous Duty Cycle Control

It should be noted such an instant attainment of the proper duty cycle for steady-state regulation is not sufficient in terms of achieving fast transient response against step input voltage change. The insufficiency is caused by the slow rate at which the filter-inductor can proceed in adjusting its minor-BH-loop operation between two input-voltage levels. This adjustment is illustrated in Figure 5, where the parallelogram ABCD represents the minor-loop operation corresponding to a given input voltage E_{i1} and a given on time T_n . In conjunction with the buck switching regulator shown in Figure 4, flux excursion ϕ_{AB} between point A and point B can be expressed as $(E_{i1} - E_0)T_n/N$ where N is the number of turns on inductor L. When E_{i1} is increased to E_{i2} in a step fashion such that $E_{i2} - E_0 = 2(E_{i1} - E_0)$, the post-transient steady-state minor loop would be A'B'C'D'. The loop is twice as tall, yet its geometrical center corresponding to NI_0 remains the same, as the load current I_0 hardly changes. What is left to be determined is the transitional details between these two parallelograms.

For clarity, it is assumed that the operation is at point A when the step change between E_{i1} and E_{i2} occurs. During T_n of the first cycle, the flux moves from A to E, where $\overline{AE} = 2\overline{AB}$. Flux returns from E to D through F during the first T_{off} , where $\overline{FD} = \overline{AE}$. The instant attainment

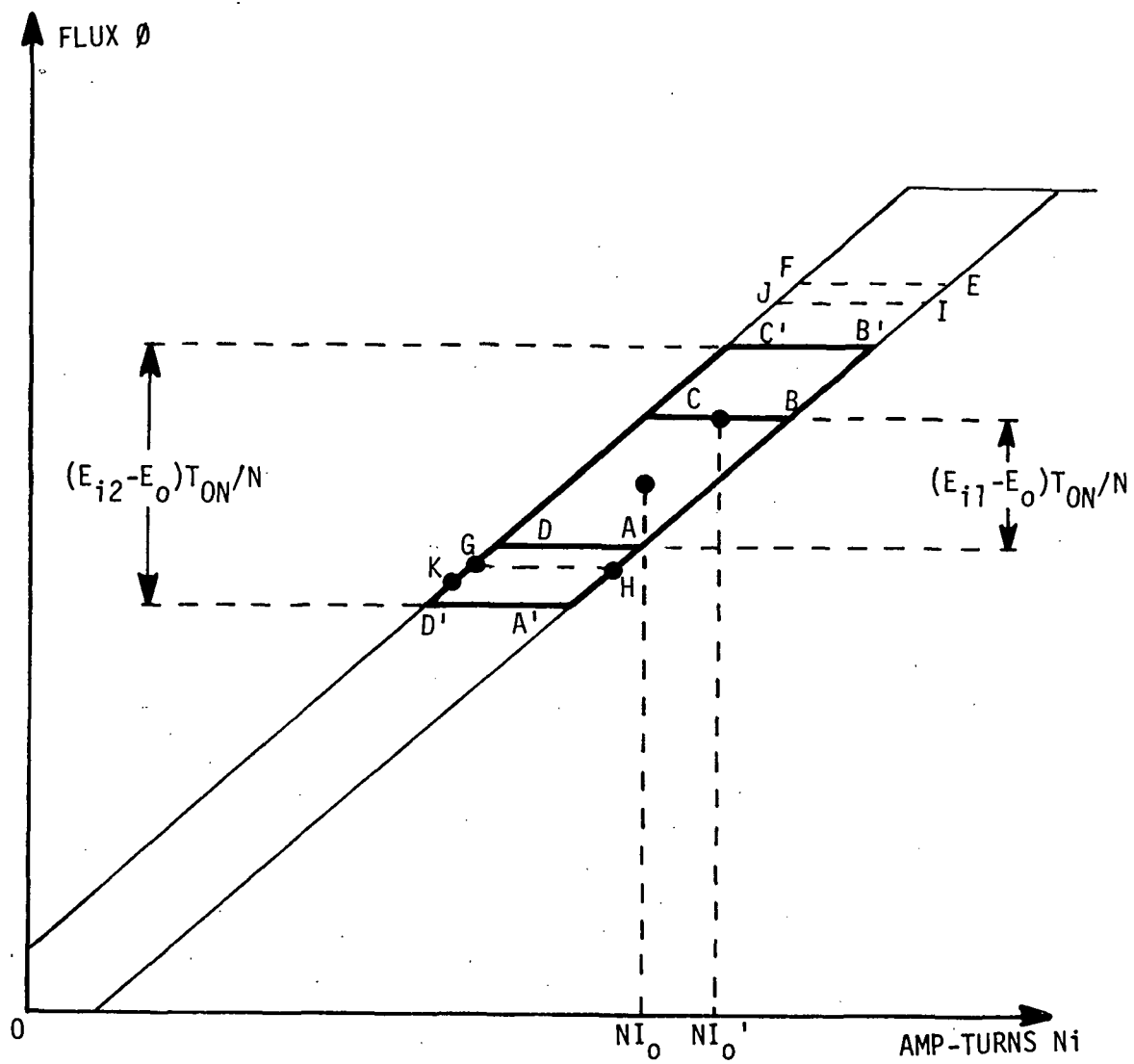


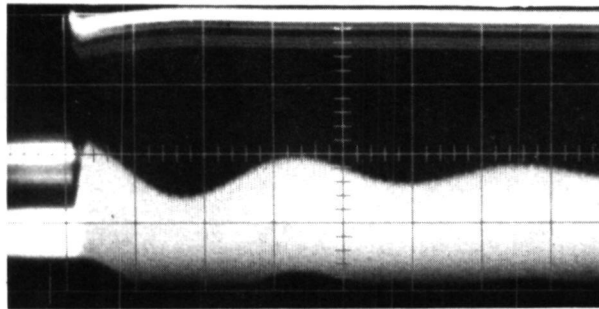
FIGURE 5. MINOR-LOOP MIGRATION OF INDUCTOR FLUX IN A BUCK REGULATOR UPON A STEP INPUT VOLTAGE CHANGE

of the proper steady-state duty cycle thus returns the flux to its starting level. However, the geometrical center of the elongated loop AEFD is now NI'_0 , which is higher than NI_0 . The energy supplied to the load is therefore higher than what is required to maintain a constant output voltage across the constant load; output voltage e_0 thus rises at a rate determined by the LCR time constant of the filter-load combination, and becomes $(E_0 + \Delta E_0)$ at the end of the first cycle. The second cycle again starts at point A, and reaches slightly lower than point E at the end of T_{on} ; the flux excursion now corresponds to $(E_{i2} - E_0 - \Delta E_0) T_n / N$. However, due to the slightly higher $E_0 + \Delta E_0$, the flux descends from about E through F to G, where G is lower than D. Following the same sequence, the third cycle flux excursion during T_{on} is HI, and is JK during T_f , where K is lower than G. It is through this slow process of mirror-loop migration that the flux will ultimately settle at its new stationary loop A'B'C'D' corresponding to an input voltage of E_{i2} .

The foregoing discussion shows that, even though the correct duty cycle is adaptively achieved in an instant manner, the dynamic response of the converter output is still handicapped by the output-filter time constant. As a matter of fact, due to the low-loss design of most output filters, the settlement of new loop A'B'C'D' can only be achieved through an oscillatory transient reminiscent of the underdamped nature of the low-frequency second-order filter. To illustrate the slow settlement, the inductor current of a constant- T_n buck regulator is shown in Figure 6A. With the step input-voltage variation shown in the upper trace, the current in the lower trace provides a true representation of the minor-loop operation of Figure 5. Due to the much lower filter frequency in relation to the switching frequency, the microscopic triangular inductor current for each switching cycle is indiscernible. The low-frequency sinusoidal envelope shared by all the switching-frequency current, however, is clearly evident.

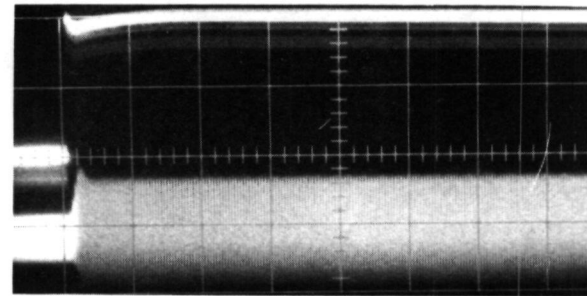
Traces of Figure 6A are expanded in Figure 6B in the vicinity of the step input change. In conjunction with the foregoing discussion, notice the return of inductor current to approximately the pre-step-change, lower-current level at the end of the first post-step-change cycle. Notice also

(A)



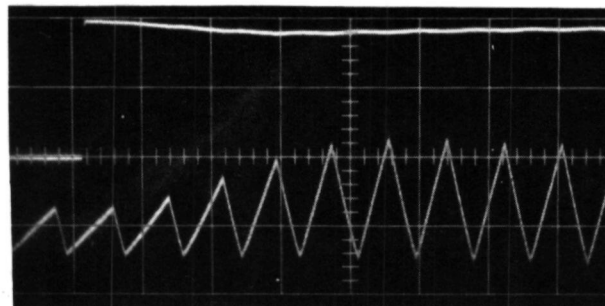
1 Amp/Division
1 ms/Division

(C)



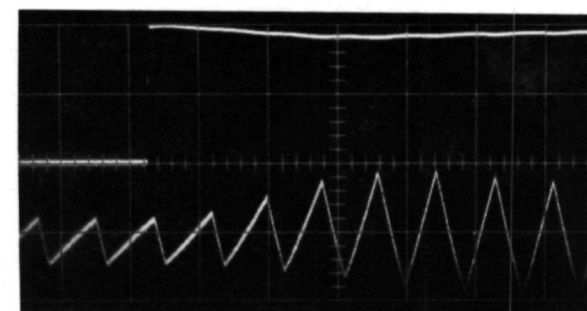
1 Amp/Division
1 ms/Division

(B)



1 Amp/Division
20 us/Division

(D)



1 Amp/Division
20 us/Division

FIGURE 6 FLUX MINOR LOOP MIGRATION WITH AND WITHOUT
THE TRANSIENT-IMPROVEMENT LOOP

the progressively descending current level at the end of each succeeding T_{off} as prescribed by the nature of the second-order filter.

It is this insight that lends a direct support for the RC compensation network first shown in Figure 3. Through this network, any rise in output-voltage E_o (e.g., after the first post-step-change cycle) brings a current proportional to $C \, de_o/dt$ into the integrator, causing the valley of the ramp voltage at the integrator output to go much lower, thus bring a much longer T_{off} and contributing to the fast attainment of converter input/output energy balance. With a properly-designed compensation the number of switching-frequency cycles required to complete the minor-loop settlement between ABCD and A'B'C'D' of Figure 7 can be greatly reduced, which results in significant improvement in the output dynamic response.

The improvement is illustrated in Figure 6C, which is the counterpart of Figure 6A with the addition of a properly-designed compensation. Notice the absence of any low-frequency oscillation in Figure 6C. Similarly, Figure 6D shows an expanded view of Figure 6C in the vicinity of the step-input-change. Transition from ABCD to A'B'C'D' is accomplished much faster than that shown in Figure 6B.

The effect of instantaneous duty-cycle attainment, therefore, has to work in unison with a quick minor-loop settlement of the energy-storage in induction in order to produce a fast dynamic response against input-voltage change. It is for this reason that the RC network shown in Figure 3 as loop 3 is needed.

One also notes the similar significance of the RC network with respect to a sudden load change. Any output-voltage transient as a result of step load change would cause the integrator-amplifier output ramp to react instantly in such a way as to quickly restore the converter input/output energy balance, thus maintaining good dynamic regulation of the converter output voltage.

4.5 IMPLEMENTATION OF DIFFERENT DUTY-CYCLE CONTROL MODES

A basic SCM objective is its capability of operating in different duty cycle control modes based on different ramp and threshold-level implementations. These modes include the following combinations of on time T_n and off time T_f :

- 1) Constant T_n , variable T_f
- 2) Variable T_n , variable T_f , variable (T_n+T_f)
- 3) Variable T_n , variable T_f , constant (T_n+T_f) , with the constant-frequency clock initiating T_f
- 4) Variable T_n , variable T_f , constant (T_n+T_f) , with the constant-frequency clock initiating T_n
- 5) Constant T_f , variable T_n .

In combination (2) where neither T_n , T_f , nor (T_n+T_f) is kept constant, a prominent design practice is for the product $E_i T_n$ to be constant, with E_i being the converter input voltage. The practice is often being referred to as line compensation, for any given input line change is met with a corresponding change in T_n such that the volt-second per cycle applied to the energy-storage element(s) is made independent of the line condition.

Implementation of these duty-cycle modes must follow certain basic rules involving regulation control and compatibility between control and protection. These rules are presented as follows.

4.5.1 Ramp-Threshold Interface*

As seen from Figure 4 on page 31, the triangular integrator output possesses a negative slope during on time T_n and a positive slope during off time T_f . In view of the fact the regulation control determines the point at which the ramp intersects the threshold level, the following conclusions become apparent:

- (A) In constant T_n , constant $E_i T_n$, or constant (T_n+T_f) duty-cycle control with the clock pulseⁿ initiating the off time, regulation is achieved by controlling off time T_f . The threshold level therefore prescribes the peaks of the triangular ramp, as the intersection of the ascending ramp with the threshold levels marks the end of the time interval T_f .

*A third category different from categories A and B described in this section involves the use of two threshold levels. Due to its special limitations, it is separately discussed in a later section, Section 5.3.1.

- (B) In constant T_f or constant $(T_n + T_f)$ duty-cycle control with the clock pulse initiating the on-time, regulation is achieved by controlling on time T_n . The threshold level therefore prescribes the valleys of the triangular ramp, as the intersection of the descending ramp with the threshold level marks the end of the on-time interval T_n .

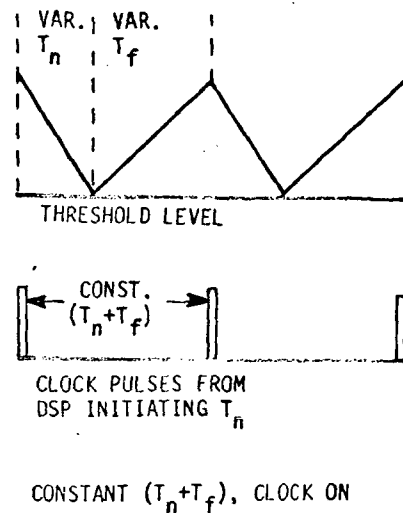
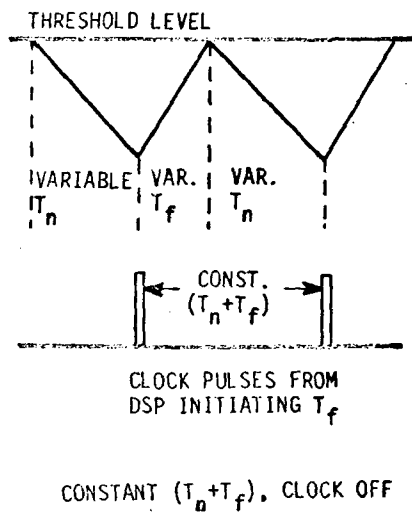
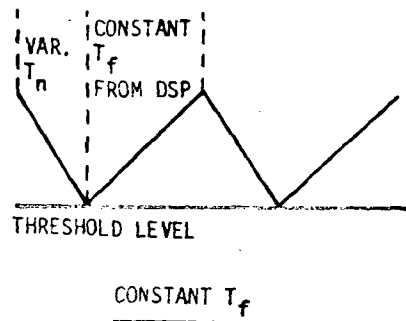
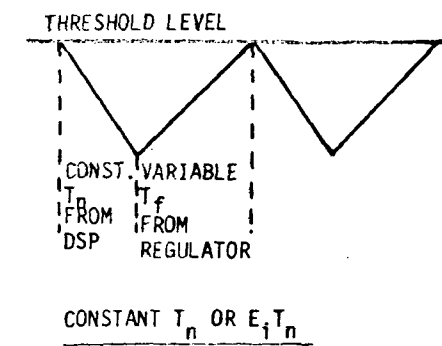
Thus the threshold level serves as either the upper or the lower boundary of the triangular ramp as a function of the duty-cycle control mode implemented. This rule governing the ramp-threshold interface is further illustrated in Figure 7.

Notice that in reality the negative-going ramp will penetrate the lower boundary threshold level somewhat. The undershoot is caused by the finite storage time of the power switch, which prolongs the negative-going ramp for the storage-time interval following the turn-off command initiated by the ramp-threshold intersection.

4.5.2 Compatibility Between Regulation Control and Peak Current Protection

As previously stated, the SCM peak-stress control is an important feature, and is achieved by limiting, on an instantaneous basis, the peak current in the power switch. Once an excessive peak current is detected, a signal is issued by the Digital Signal Processor (DSP) to immediately turn off the power switch (after a finite storage time). Since the occurrence of peak current is an abnormal operating condition invariably associated with a transient state during which the converter output regulation is non-existing, one cannot rely on the regulation control to provide the off time. The question to be resolved, then, centers on the length of the off-time interval following such a power-switch turn-off. This time interval is of practical significance. If the interval is too short, it will not allow the MMF in the energy-storage inductor (in series with the power switch) to diminish sufficiently before the next turn-on of the power switch. The consequence is a cyclic upward migration of the peak current that renders the peak-stress control ineffective.

Consequently, sufficient time must be allowed for the off-interval after each operating cycle of peak-current detection and protection. The programming of such a time interval is closely related to the ramp-threshold interface discussed in the previous section. The two categories A and B in which the threshold level serves as the respective upper and lower boundaries of the triangular ramp, are illustrated in Figure 8 for peak-current protection.



CATEGORY A

CATEGORY B

FIGURE 7 TWO MAJOR CATEGORIES OF SCM RAMP-THRESHOLD INTERFACE

In Figure 8(A), the threshold level serves as the upper boundry. Its intersection with the positive ramp marks the initiation of an on-time interval. The nominal on-time and off-time intervals during steady-state operations are shown as T_n and T_f , respectively. When a peak current is detected, say, at point a prior to the end of a nominal T_n , the T_n interval is interrupted by the peak-current protection. The power-switch turns off, and the ramp becomes positive-going. When the ramp intersects the threshold level at point b, power-switch conduction is resumed, which produces an excessive-peak-current signal at point c. The power-switch turn-off again reverts the ramp upward, resulting in the next power-switch turn-on at point d. The cyclic process occurs at a much higher frequency than that corresponding to $1/(T_n+T_f)$. The high-frequency operation at the excessive peak current is, of course, undesirable by itself. Worst yet, the inevitable storage time now becomes a significant portion of the shortened high-frequency period, thus disallowing the MMF in the energy-storage inductor to diminish properly before the next power switch conduction. Thus, after a number of cycles, the effect of peak-current protection becomes non-existing. For nominal regulation control where the threshold serves to terminate the interval T_f , the programming of a delay interval is thus needed to force an extension of the off-time interval everytime when an excessive peak current is detected. With the extended off time, the MMF in the energy-storage inductor is allowed to reset properly before the next conduction of the power switch, thereby upholding the intended utility of the SCM peak-stress control. Such a time delay has been designed into the SCM.

The counterpart of Figure 8(A) is shown in Figure 8(B). Here, the threshold level serves as the lower boundry, and its intersection with the negative ramp marks the end of the on-time interval. When a peak current is detected, say, at point a prior to the end of a nominal T_n , the ramp becomes positive going. It will not come in contact with the lower threshold level during the entire off time in the operating cycle. The length of this off-time interval is either programmed in the constant-off-time duty-cycle control, or determined by the differential $(T-T_a) > T_f$, where T is the nominal operating period of the constant-frequency duty-cycle control, and T_a is the shortened T_n corresponding to point a. Consequently, sufficient off time is always inherently provided following an excessive-peak-current detection and protection, and no provision to extend the off time is needed.

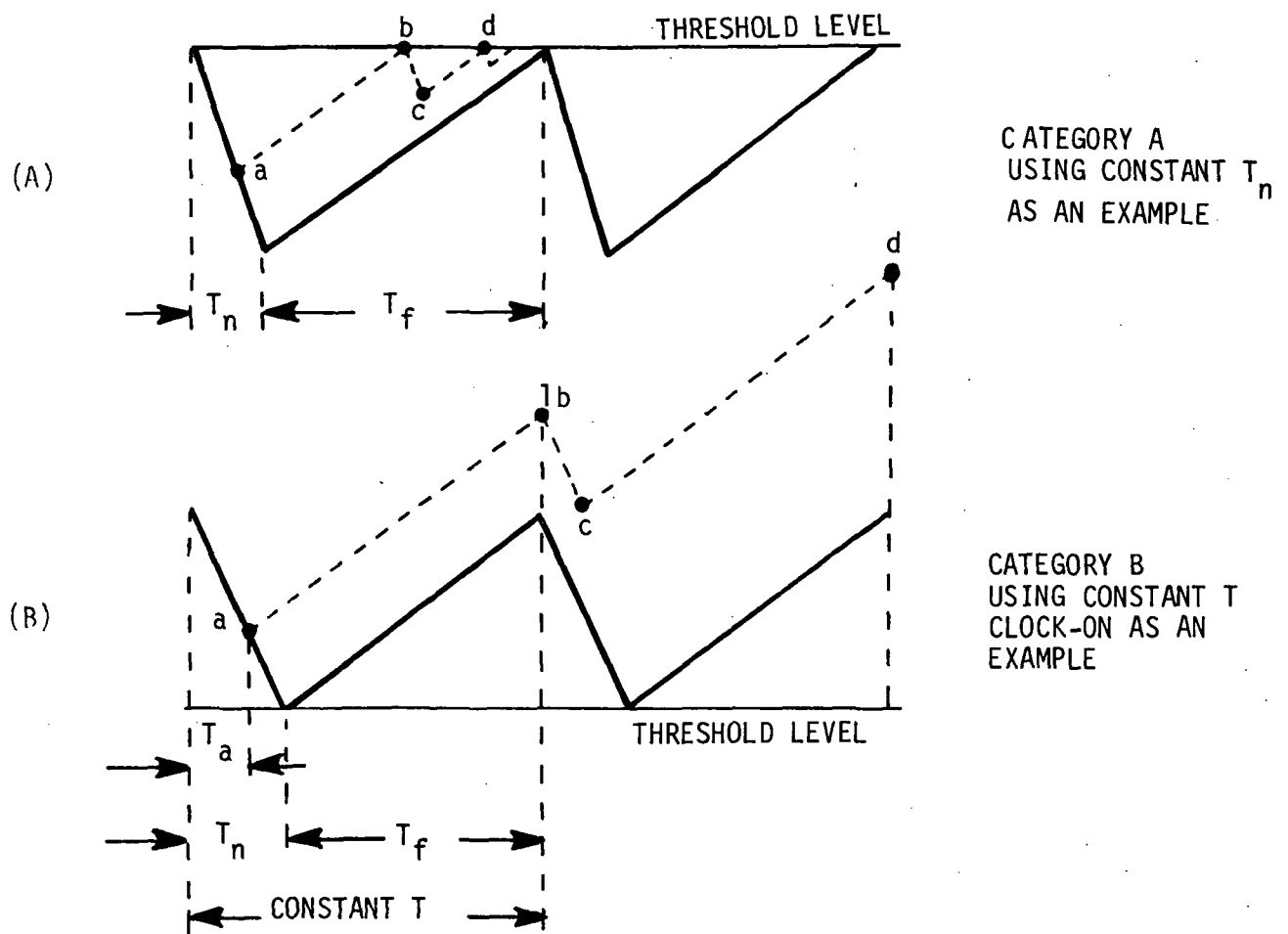


FIGURE 8. COMPATIBILITY BETWEEN REGULATOR CONTROL AND PEAK-CURRENT PROTECTION PHILOSOPHY

From the viewpoint of maintaining compatibility between regulation control and peak-stress protection, one therefore prefers the implementation shown in Figure 8(B) over that of Figure 8(A). It is for this reason that when constant $(T_n + T_f)$ duty cycle control is used, it is desirable to have the constant-frequency clock signal to initiate the on-time interval, in which case the threshold level will be used to terminate the on time.

In short, if the threshold level terminates T_n , then there is no need for an extra time delay to extend the off time following the power-switch turn-off due to peak-current protection. On the other hand, if the threshold level terminates T_f , such a delay is then necessary.

4.6 OPERATING SUBTLETY OF CONSTANT-FREQUENCY DUTY-CYCLE CONTROL

A SCM operating subtlety occurs in constant-frequency duty-cycle control, in which an instability is often observed when the duty cycle required from regulation control exceeds a certain range. Experimentally, the instability occurs when the MMF in the output filter inductor is continuous. Under this condition, the following observations can be made:

- (1) With the constant-frequency clock initiating the on time, the instability is observed when the operating duty cycle becomes larger than a certain number. In dc-dc converters where rectangular inductor voltages are sensed for ramp generation, this number is 0.5.
- (2) With the constant-frequency clock initiating the off time, the instability is observed when the operating duty cycle becomes smaller than a certain number. This number is 0.5 in dc-dc converters where rectangular inductor voltages are sensed for ramp generation.
- (3) The aforescribed instability range vanishes when the MMF in the output filter inductor becomes discontinuous, i.e., when a zero-MMF dwell-time exists in each steady-state operating cycle.

The objective of this section, therefore, is to first understand the unstable phenomenon physically and mathematically. Based on the understanding, control means to eliminate this instability is then presented.

4.6.1 Physical Understanding of Unstable Duty Cycle Range

The stability nature can be easily comprehended through graphical demonstrations. Figure 9 shows the integrator output ramp for a constant-frequency duty-cycle control, with the clock initiating the on time. Duty-cycle ratios of less and greater than 0.5 are illustrated, respectively, in Figure 9 (A) and (B). In each case, the solid line represents the steady-state waveform if a stable operation can be maintained.

The stability nature is assessed readily by examining the propagation of a small disturbance ϵ at $t=0$. The disturbance is assumed to be negligibly small so that the slopes of the triangular ramp remain unchanged.

In Figure 9(A), the disturbance is seen to diminish as the cycle propagates, and will disappear ultimately to resume steady-state operations. The steady-state operation is therefore stable. Conversely, the disturbance is seen in Figure 9(B) to diverge with the cycle propagation - an obviously unstable operation.

A closer examination reveals the basic difference between Figure 9(A) and (B). While in Figure 9(A) the less-than-0.5 duty cycle causes the ramp slope $/S_n/$ during T_n to be larger than that of $/S_f/$ during T_f , the opposite is true for Figure 9(B). Since a duty cycle of 0.5 is synonymous with $/S_n/ = /S_f/$, it is not surprising that the particular duty cycle of 0.5 indeed corresponds to stability or the lack of it.

Notice that the foregoing physical interpretation is based on the control implementation of initiating the on time by the constant-frequency clock. Such an implementation leads to a duty-cycle stability range of less than 0.5. Similar argument easily points to the conclusion that, when the clock initiates the off time, the stable duty-cycle range is greater than 0.5

4.6.2 Mathematical Proof for the Instability

A mathematical proof is provided here using Figure 9(B) as an illustration. If the steady-state ramp amplitude at $t=0$ is A , then, the equation for the negative-going ramp during on-time T_n is:

$$e_I(t) = A - S_n t \quad (1)$$

The ramp equation during off-time T_f is:

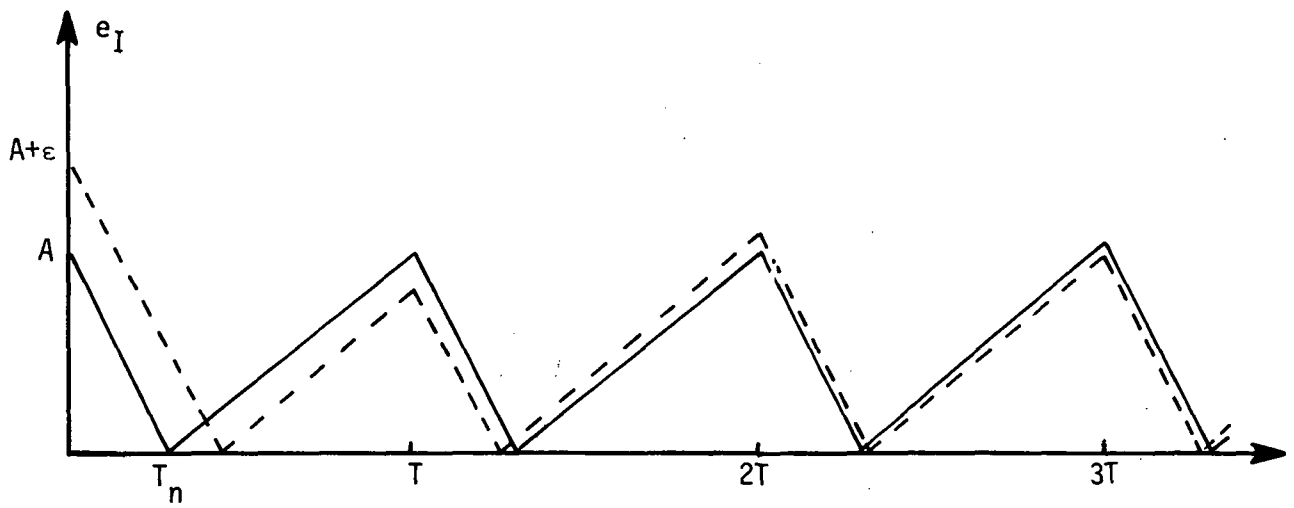
$$e_I(t) = S_f \left(t - \frac{A - E_T}{S_n} \right) + E_T \quad (2)$$

Since $e_I(t)$ of eq. (1) at $t=0$ is identical to that of eq. (2) at $t=T$,

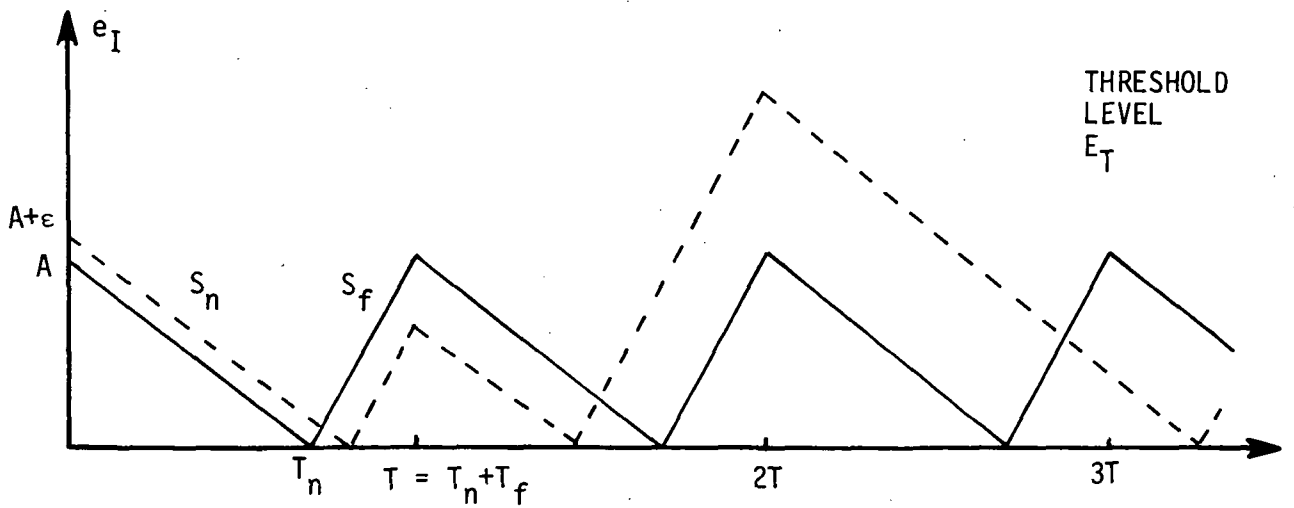
$$A = S_f \left(T - \frac{A - E_T}{S_n} \right) + E_T \quad (3)$$

If the system is subjected to a small disturbance at $t=0$, i.e.,

$$e_I(0) = A + \epsilon \quad (4)$$



(A) DUTY CYCLE LESS THAN 0.5



(B) DUTY CYCLE GREATER THAN 0.5

FIGURE 9. GRAPHICAL ILLUSTRATION OF 0.5 DUTY-CYCLE STABILITY LIMIT

Then, during T_n ,

$$e_I(t) = A + \epsilon - S_n t \quad (5)$$

and during T_f ,

$$e_I(t) = S_f \left(t - \frac{A + \epsilon - E_T}{S_n} \right) + E_T \quad (6)$$

Therefore at $t=T$,

$$e_I(T) = S_f \left(T - \frac{A + \epsilon - E_T}{S_n} \right) + E_T \quad (7)$$

Combining (3) and (7) gives

$$e_I(T) = A - \frac{S_f}{S_n} \epsilon \quad (8)$$

The error signal ϵ after propagating one cycle becomes $-\epsilon S_f/S_n$. In general, the error signal after n th cycle is therefore $\epsilon(-S_f/S_n)^n$. This relation is illustrated in Figure 10. For $S_f/S_n < 1$, a condition corresponds to a duty cycle less than 0.5, the error signal converges and eventually vanishes for a large n , thereby producing a stable system. Conversely, a greater-than-0.5 duty cycle gives $S_f/S_n > 1$, the error signal diverges, and eventually reaches a limit cycle determined by various nonlinearities within the system. The frequency of the limit cycle will be subharmonics of the switching frequency $1/T$.

It should be noted that ideal triangular waveform is assumed here to facilitate mathematical derivations. In reality, the ramp slopes are somewhat modified by the imperfect rectangular voltage at the integrator input and the additional integration of the integrator input derived from the RC transient compensation loop. Consequently, duty-cycle instability may occur at a value slightly different from 0.5.

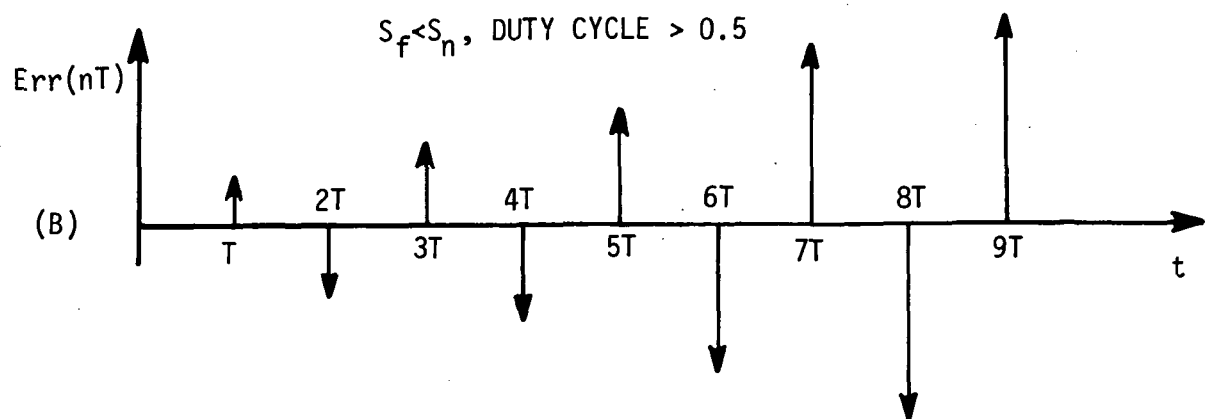
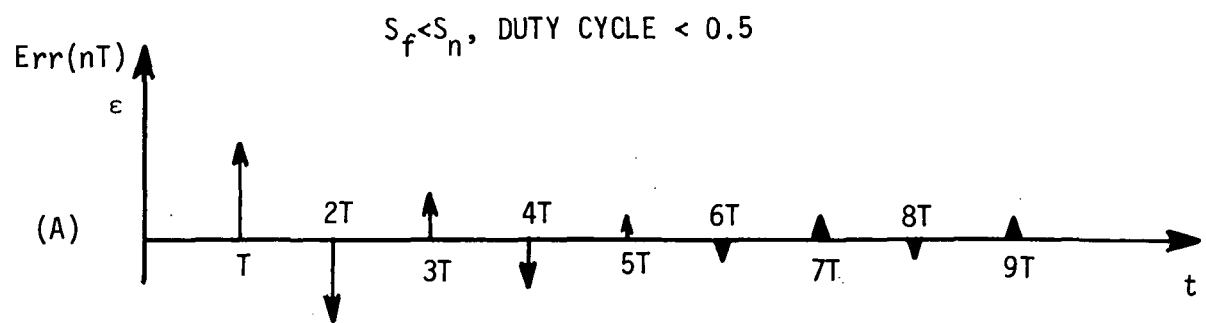


FIGURE 10. ERROR SIGNAL PROPAGATION

4.6.3 Means for Extending Stable Duty-Cycle Range in Constant-Frequency Operation

The previously-described physical interpretation and mathematical proof are not based on any particular power-stage circuit. The instability associated with the duty-cycle range thus exists for all SCM-controlled buck, boost, and buck boost configurations. This instability must be mitigated, for otherwise the utility of the SCM is seriously compromised.

There are two different remedies through which a stable constant-frequency operation can be extended to beyond the 0.5 theoretical limit. One of them resides in the redesign of the power circuit, i.e., to reduce the energy storage inductance for a given switching frequency so that a zero-MMF dwell time exists in each operating cycle. Another means is to externally force a change of the S_n/S_f ratio; the ratio was identified in the last section as the critical parameter determining the stability nature of the system. These methods are discussed as follows:

4.6.3.1 Elimination of Instability through Discontinuous Inductor MMF Operation

When the inductor MMF becomes discontinuous, a steady-state operating cycle contains three distinct time intervals. These intervals are shown in Figure 11(A). The cycle starts with a zero MMF in the inductor, and the MMF increases during on-time T_n . Off-time T'_f follows, and the MMF decreases to zero at the end of T'_f . During the interval $T''_f = T - (T_n + T'_f)$ where T is the constant-frequency period, the MMF remains zero until the initiation of the next on-time T_n . The corresponding inductor voltage is shown in Figure 11(B). During interval T''_f , there is no voltage across the inductor. As a consequence, the integrator output voltage resembles that of Figure 11(C), in which a constant-voltage plateau coincides with the time interval T''_f . In Figure 11(D), a disturbance ϵ is presented to the integrator ramp. It is the objective of this section to provide a mathematical proof that the error ϵ does not diverge as the cycle propagates, thus maintaining a stable operation regardless of the operating duty cycle of the system.

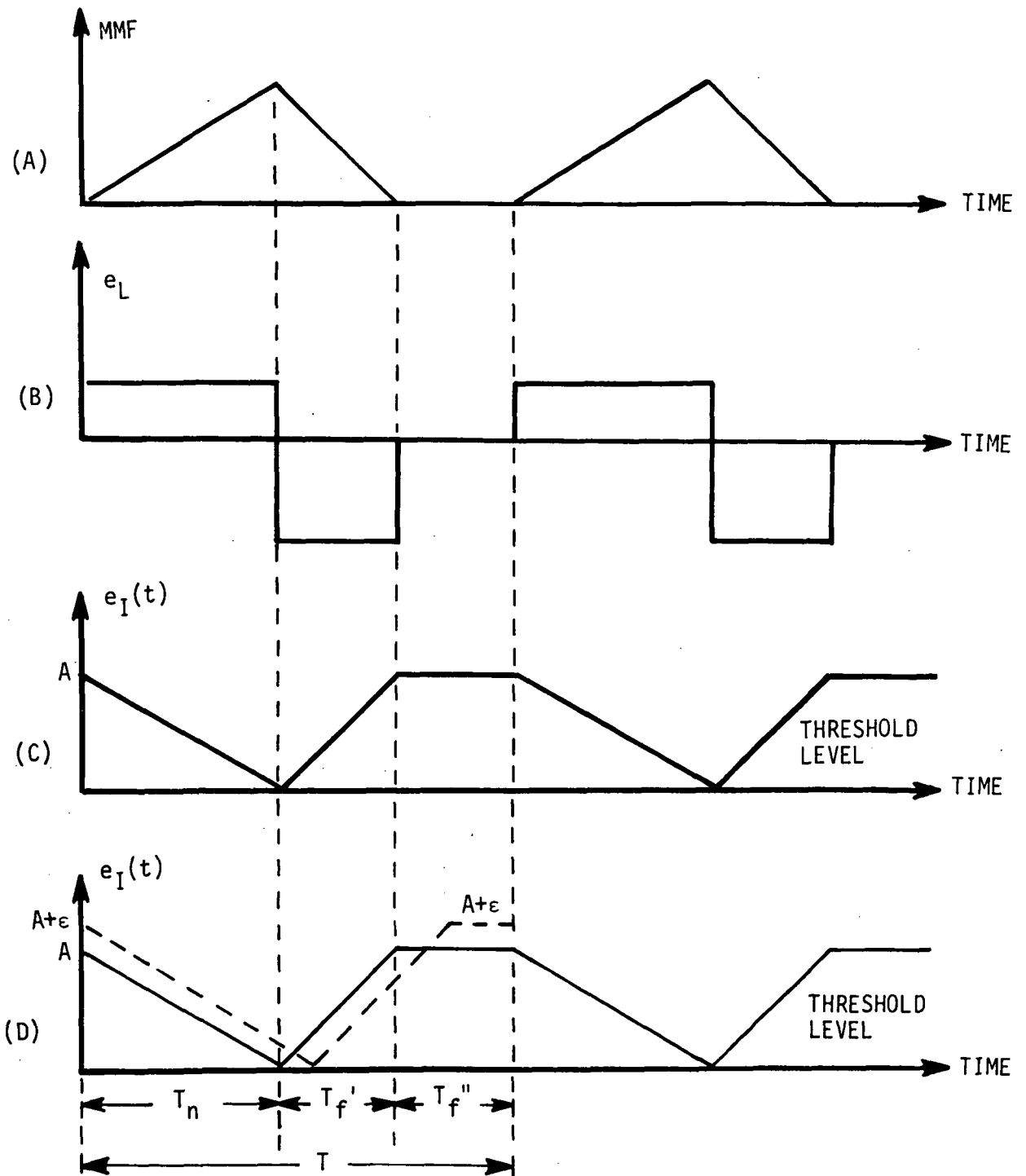


FIGURE 11. DISCONTINUOUS INDUCTOR MMF OPERATION

Referring to the steady-state operation shown in Figure 11 (C), equations for the triangular ramp during T_n and T_f' are, respectively, the following:

$$e_I(t) = A - S_n t, \quad (9)$$

$$e_I(t) = S_f(t - T_n) + E_T \quad (10)$$

from (9), at $t=T_n$,

$$T_n = \frac{A - E_T}{S_n} \quad (11)$$

Furthermore, the volt-second balance of each operating cycle during T_n and T_f' demands that

$$T_f' = K_1 T_n, \quad (12)$$

when K_1 is a function of converter input and output voltages as well as the turns ratio between primary/secondary winding. Substituting (11) and (12) into (10), then, at $t=T_n+T_f'$, one has:

$$[e_I(t)]_{\text{at } t=T_n+T_f'} = S_f K_1 \left(\frac{A-E_T}{S_n} \right) + E_T \quad (13)$$

This amplitude represents the integrator output level at both $t = T_n+T_f'$ and $t = T$, for a zero slope exists during the entire interval T_f'' .

If the integrator output is subjected to a small disturbance ϵ , following a similar derivation one has:

$$[e_I(t)]_{\text{at } T=T_n+T_f'} = S_f K_1 \left(\frac{A-E_T}{S_n} + \frac{\epsilon}{S_n} \right) + E_T \quad (14)$$

Comparing (13) and (14) reveals the propagation of ϵ from one cycle to the next to be $K_1 \epsilon S_f / S_n$. However, steady-state operation of Figure 11(C) clearly shows that

$$S_f/S_n = T_n/T_f' \quad (15)$$

Consequently, the propagation of disturbance ϵ from one cycle to the next becomes $K_1 \epsilon S_f/S_n = \epsilon$. The disturbance is non-divergent, signifying a stable operating system.

Again, the derivation here is general, and holds true for all basic buck, boost, and buck boost power configurations. Notice also the abrupt change from unstable, continuous-MMF operation (Figure 9B) to stable, discontinuous-MMF operation (Figure 11D). This property has always been observed experimentally.

While the discontinuous-MMF operation is a sure way to extend stable operation to all duty cycles, practical considerations such as high peak power-switch current, source EMI, and output filtering often preclude this operation from the intended design, particularly when the converter power rating is high. Consequently, the discontinuous-MMF operation cannot be regarded as a general stabilizing means for all applications.

A more general method of extending stable duty-cycle range while allowing both continuous- and discontinuous-MMF operations is discussed below. The method was substantiated through its successful deployment in the deliverable demonstration breadboards.

4.6.3.2 Extension of Stable Duty Cycle Range by External Ramp Addition

An alternate means to mitigate the duty-cycle instability is to perturb the ratio of S_n/S_f in extending the range of stable operation.

As previously stated, when the constant-frequency clock initiates T_n , the system becomes unstable when the duty cycle exceeds 0.5, which corresponds to $S_n/S_f < 1$. On the other hand, when the clock initiates T_f , the system becomes unstable when the duty cycle is below 0.5, which corresponds to $S_n/S_f > 1$. The stabilizing external ramp must therefore be added such that $S_n/S_f > 1$ with clock initiating T_n and $S_n/S_f < 1$ with clock initiating T_f . For illustration, the former case is discussed as follows. Basically, the intended ramp addition is to cause the descending slope during T_n to be steeper than the ascending slope during T_f even when the duty cycle is greater than 0.5.

An example of such an implementation is graphically illustrated in Figure 12. Here, an external ramp of slope S_e is added to strengthen slope S_n during T_n . The external ramp slope S_e has to satisfy the inequality:

$$S_e > (S_f)_{\max} - (S_n)_{\min}$$

Since the largest differential between $(S_f)_{\max}$ and $(S_n)_{\min}$ invariably occurs at the minimum input voltage, the slope S_e must be sufficiently large to stabilize the minimum input-voltage operation, which corresponds to the maximum duty cycle.

The utility of this external ramp function has been substantiated experimentally for buck, boost, and buck boost power configurations. However, the audio-susceptibility performance of the converter is degraded somewhat in the presence of such an external ramp. Ideally, what one needs is a S_e that is just sufficient to perform its stabilization function. Since an S_e designed to stabilize a low input-voltage operation is more than sufficient at higher input voltages and therefore incurs the attendant audio-susceptibility performance reduction, an external ramp with a variable slope S_e is implemented in the SCM. The variable slope varies inversely with the input voltage, having the steepest slope when it is needed most, i.e., when the input voltage is at its minimum.

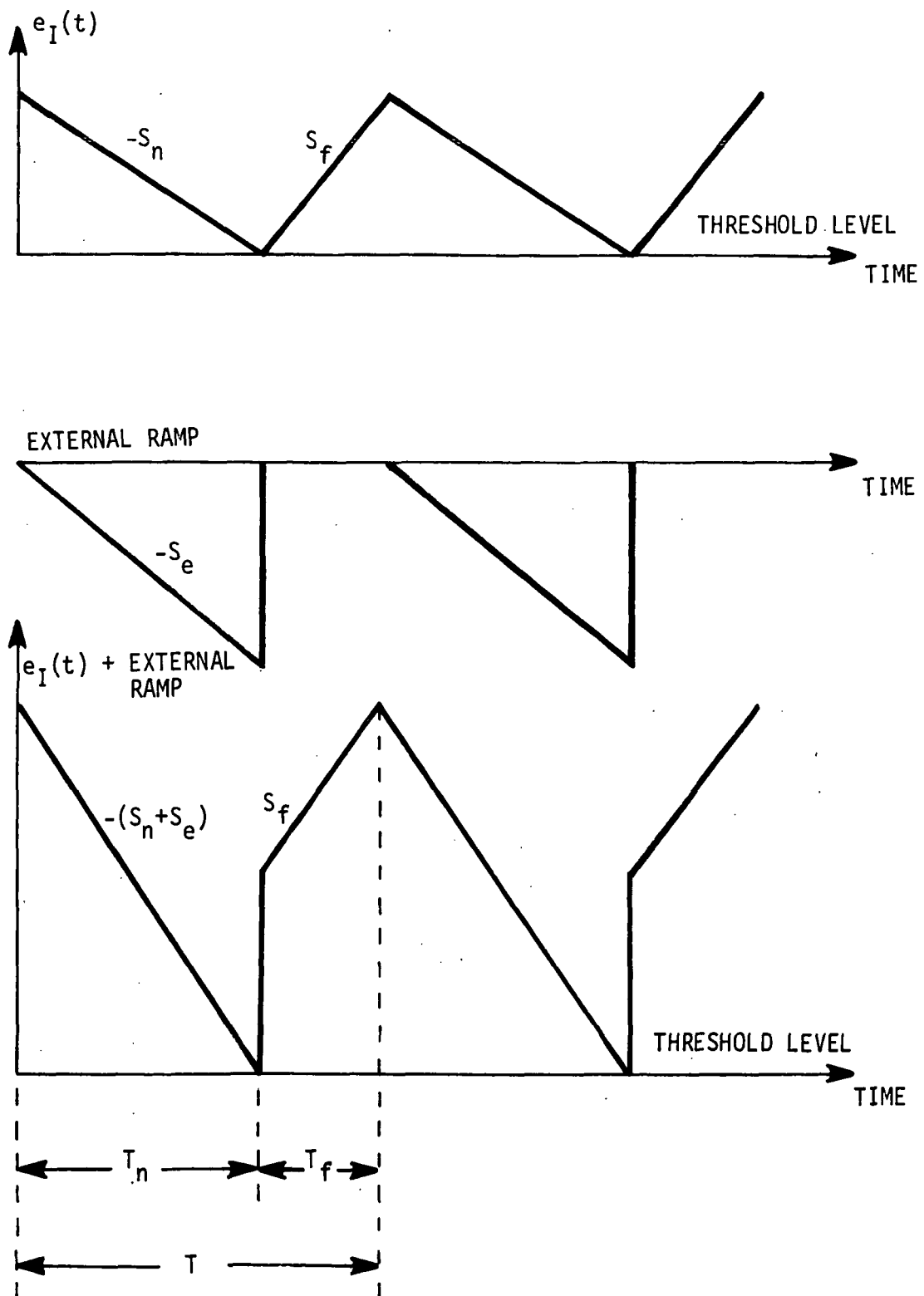


FIGURE 12. EXTENDING CONSTANT-FREQUENCY STABLE DUTY-CYCLE LIMIT THROUGH EXTERNAL RAMP ADDITION

5. THE DIGITAL SIGNAL PROCESSOR (DSP)

As previously stated in Section 3.4.4, the DSP is the nerve center of the control system, as it must process all incoming control signals and transmit the correct output signal to operate the power switch.

The signals processed by the DSP encompass control signals and protection/command signals. Control signals include:

- Regulator Control
- Duty Cycle Implementation
- Minimum Off-Time Control
- Control Circuit Input/Output Isolation

Command/Protection signals include:

- Peak Stress Protection
- Power Stage Turn-off Shutdown
- On/Off Command

To incorporate these controls, the DSP must contain certain basic functional blocks. In the following sections, these blocks are first identified. Different combinations of these functional blocks to form various duty-cycle control modes are then presented. A common schematic capable of implementing these control modes is given, and component evaluation of digital logics is discussed.

5.1 BASIC BUILDING BLOCKS FOR THE DSP

To effect a DSP, the basic building blocks consist of the following elements:

- Isolator
- Time Delay
- Memory
- Oscillator
- Control NAND Gate
- Power/Control Interface

The function of the isolator is to provide the control circuit input/output isolation, which is often a specified requirement. By necessity, the Analog Signal Processor sensing regulating error is ohmically coupled to the converter output. The DSP, however, must be coupled to the converter input so as to remain operational even when the converter output is short circuited. It is for this reason that the isolator block is best located between ASP and DSP. The output of the ASP is the regulator control signal, to which the isolator is electrically connected. As stated previously, the ASP regulator control signal appears only as a pulse carrying no analog or time information, as it only serves to initiate the on-time or the off-time interval to be determined by the DSP. Consequently, the isolator does not need an undue emphasis on its signal transmission fidelity other than that the transport lag should be negligibly small in relation to the switching frequency of the converter.

The time-delay is needed to implement on time T_n in the case of constant T_n , or constant $E_i T_n$ control. It is also needed to implement the minimum off time following termination of each conduction interval when the peak-current protection is effective. Two guidelines are imposed on the generation of these time intervals to minimize noise susceptibility: (1) All timing signals are dc coupled, with no ac or capacitive coupling for digital pulses, and (2) wherever practical, controlled time intervals are mechanized using passive parts instead of regenerative pulse generators.

The memories are basically flip-flops used to effect logical state changes as a result of various input control signals.

The oscillator produces clock signals in constant-frequency duty cycle operations. It also interfaces with synchronization signals when the converter is sinked with an external constant-frequency clock.

The control NAND's are used to gate logic signals. From a component viewpoint, the aforementioned memory block is simply NAND gates cross-connected in a positive-feedback mode to maintain memory data.

The power control interface maintains electrical compatibility between the control circuit and the power-switch basedrive of the power circuit. (See Fig. 2, p. 19).

There are various ways through which these different functional blocks can be interconnected to form a DSP performing different duty-cycle control modes. Some illustrative examples are given in the next section.

5.2 DSP BLOCK DIAGRAMS

To illustrate combinations of basic functional blocks to form different DSP's, two duty-cycle control modes are shown in Figures 13 and 14, for constant - T_{on} (or, constant - $E_i T_{on}$) and constant frequency, respectively.

5.2.1 Constant - T_{on} Duty Cycle Control

The processing of digital signals in Figure 13 is explained by key points identified as points 1 through 12. To start with, it is assumed that regulator control signal 9 (through isolator as previously discussed) is always logical-1, a condition equivalent to no regulator action (i.e., the output voltage is lower than regulator reference).

When signal 9 is logical-1, the blocks in Figure 13 except for the power-interface blocks are combined to form a free-running oscillator. The oscillating frequency depends on whether the peak-current protection signal 10 is a logical-1 or logical-0. Taking the converter command-on for illustration, it will take a few cycles of current build-up before the peak current in the energy-storage inductor reaches the predetermined protection level. Thus, prior to reaching this limit, signal 10 is a logical-1, time delay T_p is not actuated by the peak-current sensor, and the oscillating frequency of the DSP is determined by $1/(T_n + T_m)$ where T_n sets the on time and T_m sets the minimum off time of the converter. These time intervals are coupled to the base drive circuit to control the power switch through the power-interface block.

For practically all converter designs, the predetermined peak-current protection level will be reached before the converter attains an output level corresponding to the regulator reference. During this interval of converter-output buildup, regulator signal 9 remains logical-1, while peak-current signal 10 becomes logical-0 in each cycle before the nominal T_n is timed out. Time delay T_p is activated, which shortens T_n to T'_n and replaces T_m with $T_p \geq T_m$. The operating frequency during this time interval of output-voltage buildup is thus $1/(T'_n + T_p)$.

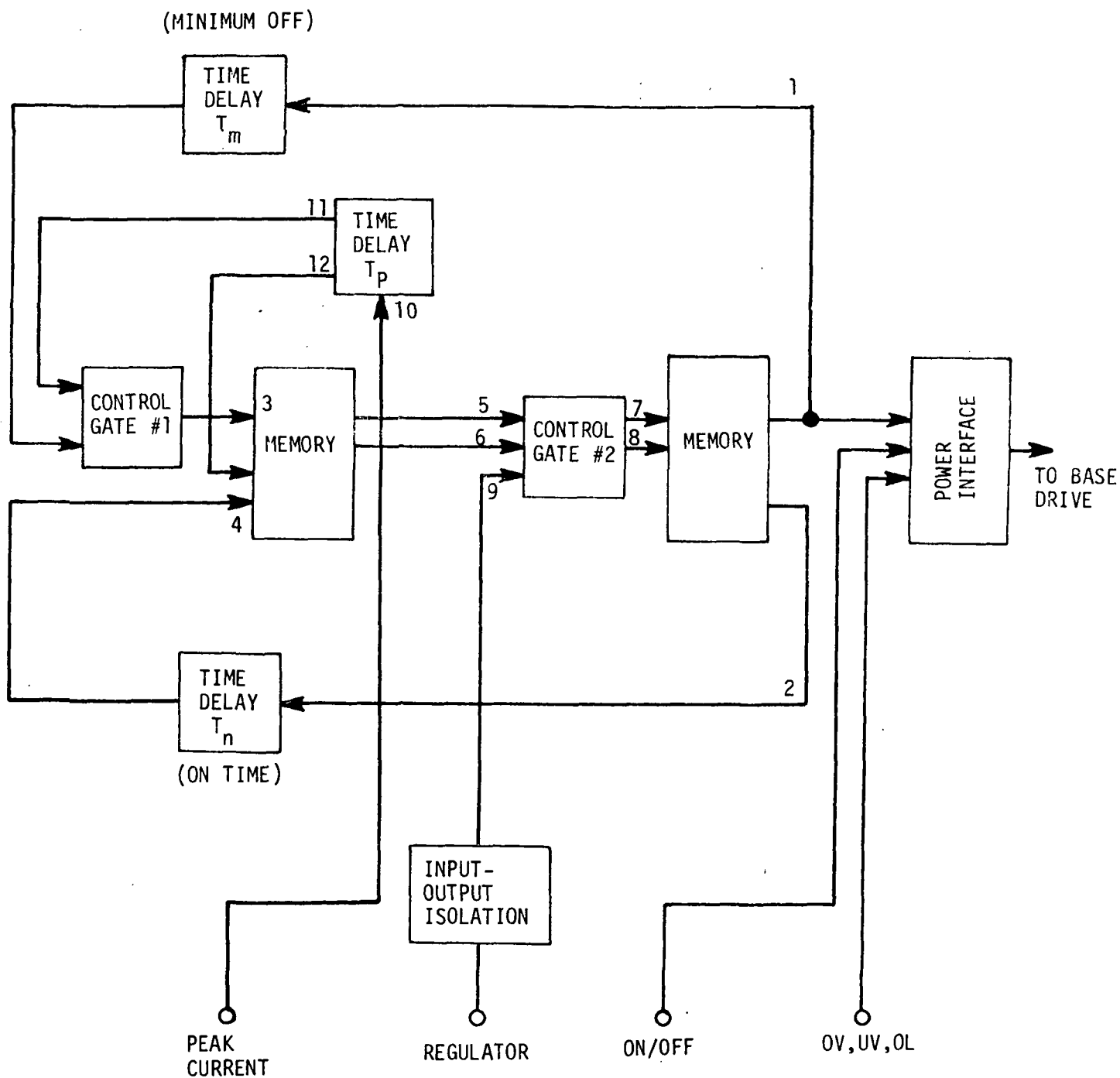


FIGURE 13 BLOCK DIAGRAM FOR A CONSTANT- T_n (or $E_i T_n$)
DIGITAL SIGNAL PROCESSOR

Eventually, the converter reaches its intended regulation level. Steady-state triangular ramp begins to intersect the threshold level in each cycle. Proper power and control circuit design ensures signal 10 to be always logical-1, and signal 9 to exhibit logical-0 and logical-1 in accordance with the ramp-threshold interface described in the previous section. When signal 9 goes logical-0, signal 7 is forced to go logical-1. On-time T_n and minimum-off time T_m are still timed out normally. However, because signal 9 is maintaining signal 7 at logical-1, the change of state in signal 5 is not registered in signal 7. Thus, minimum-off-time T_m is disabled, and the output signal 1 is now a longer time interval determined by the regulator action. Representing this interval as T_f , the converter frequency as controlled by the DSP becomes $1/(T_n + T_f)$.

The converter on/off command signal and the converter shut-off signal, the latter can be caused by converter output overvoltage, input undervoltage, or output persistent overload, are processed by the power interface block. These signals respond to either external command or internal protection for the initiation or the termination of the converter operation. A logical-0 input always terminates the operation, and reset is required before restart.

Due to the latching function associated with the OV, UV, and OL shut-off, these signals are normally processed by another memory block before entering the power interface. This is different from the peak-current signal and the regulator signal, which are required to exhibit both logical-0 and logical-1 cyclically. Consequently, the regulator signal 9 and the peak-current signal 10 are generally obtained from a threshold detector.

5.2.2 Constant-Frequency, Clock-On Duty Cycle Control

The constant-frequency DSP, with the clock initiating the on time, is shown in Figure 14. It processes the same signals as those of Figure 13. However, the existence of an oscillator defining a constant on time plus off time under all circumstances enables the regulator signal to determine both T_n and T_f in Figure 14. The time-delay block T_n shown in Figure 13 is thus eliminated. Furthermore, section 4.5.2 has fully justified in the constant-frequency, clock-on control the elimination of time-delay T_p of Figure 13 following an excessive-peak-current detection. Excluding these blocks along with their attendant control gates results in the simple block diagram shown in Figure 14.

The operating frequency determined by the DSP is a constant T . During the time when the peak-current protection is inactive and the converter output is below the reference, the off time as determined by the DSP is T_m . During the time when peak-current protection is active and the converter output is below reference, the off time is $(T - T'_n)$, where T'_n is the prematurely-terminated on time due to the peak-current protection. When the converter output is regulated at the reference level, the off time is $(T - T_n)$, where T_n is the on time prescribed by the regulator signal.

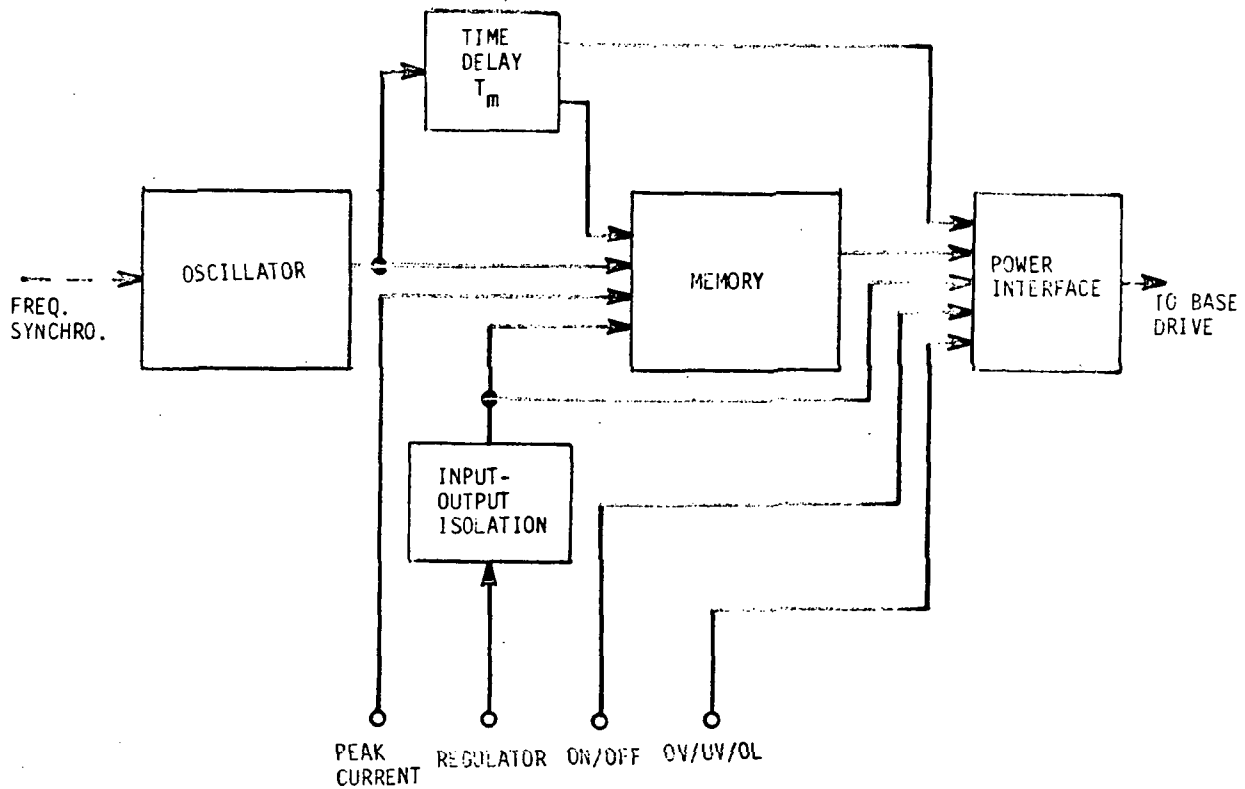


FIGURE 14 . BLOCK DIAGRAM FOR A CONSTANT-FREQUENCY DIGITAL SIGNAL PROCESSOR

5.3 A COMMON SCHEMATIC DIAGRAM FOR DIFFERENT DSP'S

Discussed in this section is the circuit implementation of different duty-cycle control modes based on a common schematic diagram. Different duty-cycle controls are made possible through different connections. Before engaging the details concerning these controls, it is worthwhile at this juncture to consider briefly the impacts of these controls to power and control circuit performances.

5.3.1 Duty-Cycle Control Types and Impacts to SCM Implementation

The following duty-cycle control types in SCM applications are easily categorized by their ramp-threshold interfaces previously discussed in Section 4.5:

- (A) The threshold level prescribes peaks of the triangular ramp.
- (B) The threshold level prescribes valleys of the triangular ramp.
- (C) Two threshold levels prescribe peaks and valleys of the triangular ramp.

Category (A) includes constant- T_n , constant- $E_i T_n$, or constant- $(T_n + T_f)$ duty-cycle control (with the constant-frequency clock initiating the T_f interval). It is an essential category as the constant- T_n duty cycle inherently serves as the basic control scheme for an important class of high-power dc-dc converters, namely, the power processors which rely on the LC series-resonant phenomenon to accomplish the power inversion where the on-time pulse interval is fixed for a given LC design. Consequently, category (A) is included in the control-circuit demonstration for this program phase. Although the series-resonant converters are the basis of such an inclusion, one must not lose sight of the fact that for other conventional dc-dc converters such as buck, boost, and buck-boost types, the selection of constant- $E_i T_n$ over constant- T_n for duty-cycle control is always advantageous from the viewpoint of converter performance. For a given weight and loss, performance characteristics such as source EMI, output ripple, peak current for a given line/load range, and audiosusceptibility, are invariably improved when constant- $E_i T_n$ instead of constant- T_n is used. The constant- $E_i T_n$ control is selected to demonstrate control category (A) in this program phase.

Category (B) includes constant- T_f and constant- (T_n+T_f) duty-cycle control (with the constant-frequency clock initiating the T_n interval). In these two control types, the constant- T_f control has yet to gain any popularity due to its potential limitation in converter starting. The limitation becomes real when the shortened on time caused by peak-current protection is associated with a constant off time to form a duty cycle too small to allow the converters output to build up to its intended regulation level. While this limitation is practically nonexistent for buck converters whose outputs derive energy during both T_n and T_f , it is serious for buck boost converters whose outputs derive energy from the energy-storage inductors only during T_f , with the inductors receiving energy from converter inputs during T_n . An insufficient T_n , in conjunction with a constant T_f , generally results in the failure of the converter output to reach its regulation level. For this reason, the constant- T_f control is considered to suffer from a lack of the required universality, and is not included as a preferred approach. Constant-frequency duty-cycle control, with the clock initiating T_n , is therefore selected to demonstrate control category (B) in this program phase.

Category (C) includes the use of two threshold levels to determine both T_n and T_f intervals. SCM development based on this approach has revealed the following operating limitations:

- The converter frequency is highly dependent on converter output ripple, power-switch storage time, and key control component parameters, making control-circuit adjustment for performance optimization extremely difficult.
- The control is difficult to incorporate an orderly peak-current protection, as neither T_n nor T_f is well defined when the output voltage is lower than the reference (i.e., when the integrator output is above the upper threshold level).
- The control cannot be easily adopted to discontinuous-inductor-current operation.

Due to these limitations, category (C) is not regarded as a preferable approach; it is not included for demonstration.

Consequently, a common schematic design is conceived in this program phase to demonstrate the constant- $E_i T_n$ duty cycle of control category (A) and the constant-frequency duty cycle of control category (B). The schematic diagram is presented next.

5.3.2 Common Schematic Diagram for Different DSP's

The circuit implementations of the constant- $E_i T_n$ DSP and the constant-frequency DSP are shown in Figures 15(A) and (B), respectively. Other than differences in wire connections, the two DSP's contain identical component parts.

5.3.2.1 Constant T_n or Constant $E_i T_n$ DSP

Various components of Figure 15(A) are grouped physically in relation to the constant - $E_i T_n$ DSP block diagram shown previously in Figure 13. A quad-threshold-detector, consisting of U1A to U1D, is used to configure TIME DELAYS for minimum off time T_m and constant on time T_n . A constant voltage, V_{CC} , is used as the dc supply for the entire DSP. This voltage is also divided down by R6 and R7, and used as the reference voltage for all threshold detectors. The reference voltage, along with U1A, U1B, V_{CC} , and the charging of C1 through R1, determines T_m . Likewise, the reference works in conjunction with R2, C2, U1C, U1D, and V_{CC} to determine T_n . Depending on whether R2 is being supplied from V_{CC} or from converter input voltage E_i , the T_n interval can be either a fixed T_n or a T_n that varies as an inverse function of E_i , i.e., a constant $E_i T_n$. Resistors R4 and R5 serve to discharge C1 and C2, respectively, following the termination of T_m and T_n . Resistances for R4 and R5 are much smaller than R1 and R2 to effect fast discharges for C1 and C2.

TIME DELAY T_p subsequent to each peak-current detection is provided by U2 and the time constant effected by $R_3 C_3$. The time delay is actuated by a logical-0 signal from the peak-current sensor feeding pin 2 of U2. Such a signal causes the output pin 3 of U2 to go logical-1 and pin 10 of the hex-inverter U7 to go logical-0 for a time interval T_p . As indicated in the block diagram of Figure 13, signals prescribing time-delay intervals T_m and T_p are fed to a CONTROL GATE (1). In Figure 15(A), the CONTROL GATE is represented by U3A.

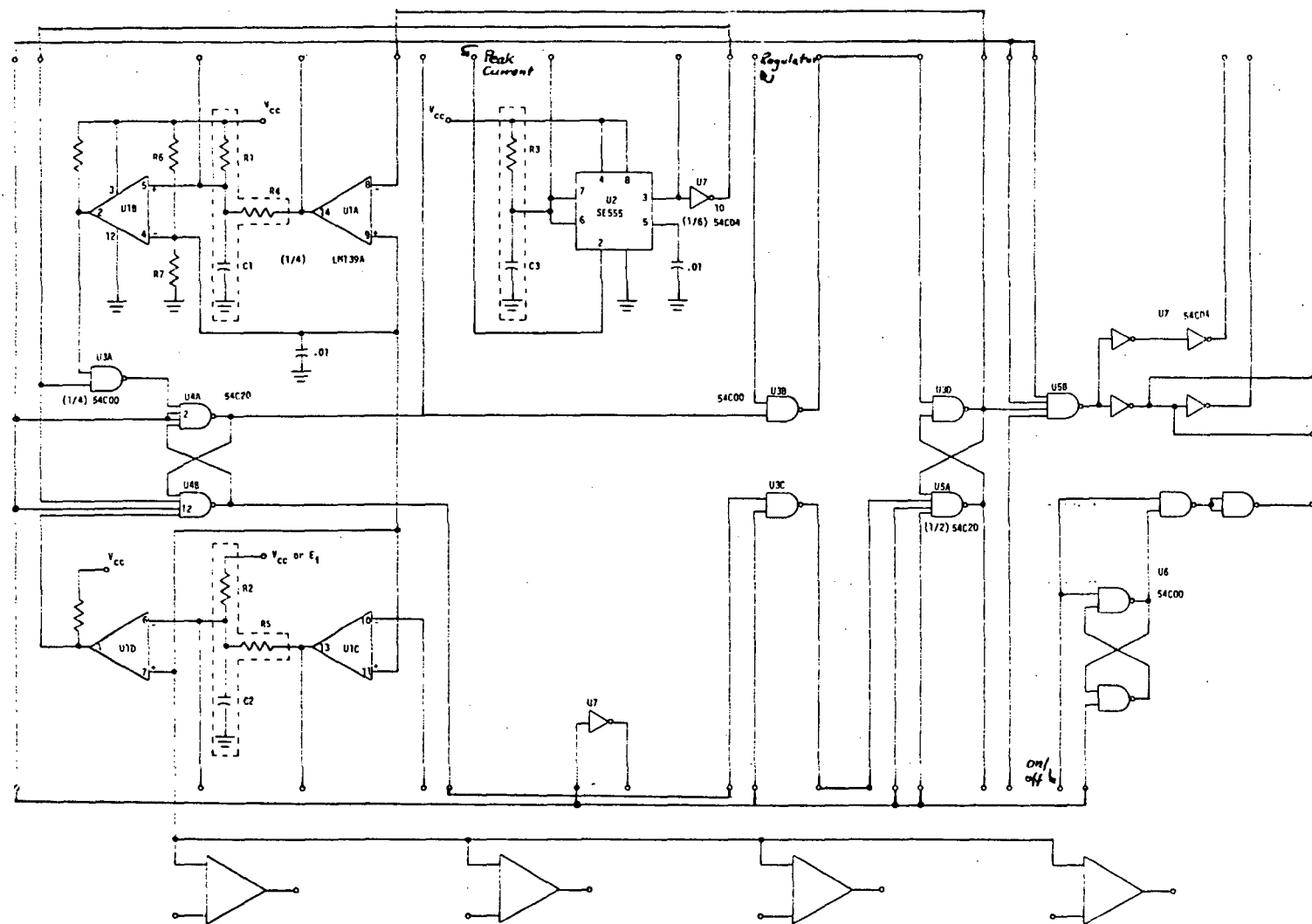


FIGURE L15(A) SCHEMATIC DIAGRAM OF A CONSTANT- $E_i T_n$ DIGITAL SIGNAL PROCESSOR

MEMORY (1) of Figure 13 is implemented through U4 in Figure 15(A) connected as a flip-flop. In addition to receiving all input signals indicated in Figure 13, each of U4A and U4B has at least one spare input (e.g., pin 2 of U4A and pin 12 of U4B). These two pins can be used when the DSP is required to synchronize with an external clock.

CONTROL GATE(2) of Figure 13 is represented by U3B and U3C in Figure 15(A). In addition to processing signals from MEMORY (1), it also receives the regulator signal as previously stated.

MEMORY (2) function is carried out by U3D and U5A cross-connected as a flip-flop. The quad inputs of U5A are not fully utilized in the constant- $E_i T_n$ DSP; they are needed for constant-frequency DSP to be discussed later.

POWER INTERFACE is accomplished by U5B, U6, and U7. Similar to U5A, input pins to U5B are not fully utilized in constant- $E_i T_n$ control. The function of U6 is to accommodate the on-off command and converter OV, UV, or OL shut-off; a flip-flop memory is therefore included. The interface function is enhanced by U7, which provides the flexibility of using either a logical-0 or logical-1 signal to effect the control of the power-switch base drive.

Since protection signals including peak-current detection, UV, OV, and OL are in the form of "logical-0" or "logical-1", which corresponds to "protection needed" or "no protection warranted," outputs from sensors of peak-current, UV, OV, and OL must be processed by threshold detectors. Depending on the accuracy required, these threshold detectors can be either crude or precision types. Furthermore, certain protections such as peak-current and OV require fast responses without delay, while others such as UV and OL desire some built-in time delay to avoid any false triggering. In Figure 15, four precision detectors are provided for the various protection functions. The extent and the details of their utilization in a specific application are at the complete discretion of a SCM user.

Notice the dotted boundaries for R1-C1, R2-C2, and R3-C3 in Figure 15(A). The values of these components determines the basic operating frequencies of the converter during nominal as well as transient operations. As such, they are to be designed by the SCM users. Consequently, those components within the dotted boundaries are physically external to the SCM, thus allowing a user to select the operating frequency for a given design regardless the duty-cycle control mode implemented for the DSP.

5.3.2.2 Constant-Frequency DSP

Various components of Figure 15(B) are grouped physically in relation to the constant-frequency DSP block diagram shown previously in Figure 14. The OSCILLATOR can be either free-running through U1, V_{CC} , R1, R2, R4, R5, C1, C2, and U4, or it can be synchronized to external clock signals applied to pin 2 of U4A and pin 12 of U4B. Notice the output of U4 feeds U1A and U1C directly producing an oscillating frequency unperturbed by the regulator signal or the peak-current protection signal. On-time T_n is initiated by the leading edge of the clock pulse going from logical-1 to logical-0. In order to allow extremely-small duty cycle operation, the clock pulse is configured very narrow in width. With the memory output no longer feeding CONTROL GATE (2), the gate is not needed in the constant-frequency DSP.

As previously stated, a constant-frequency clock-on DSP does not need any time delay following an excessive peak-current detection. Thus the U2 used in Figure 15(A) for implementing T_p is used here in Figure 15(B) for implementing TIME DELAY for minimum off time T_m . Essentially, the T_m interval represents the difference between the period of the OSCILLATOR and the time interval determined by U2 in conjunction with time constant R_3C_3 . Immediately preceding the T_n interval, interval T_m makes its presence known only when the converter output is below the regulation reference. The regulator signal only extends the off time to produce the desired duty cycle. The rest of the circuit is similar to that of the constant- E_iT_n DSP previously described.

5.3.3 Digital Logic Component Evaluation

Digital logic NAND gates evaluated include High Threshold Logic (HTL), Transistor-Transistor Logic (TTL), and complementary MOS (CMOS). Breadboards for evaluation purposes were built. The relative merits of these logic types are summarized as follows:

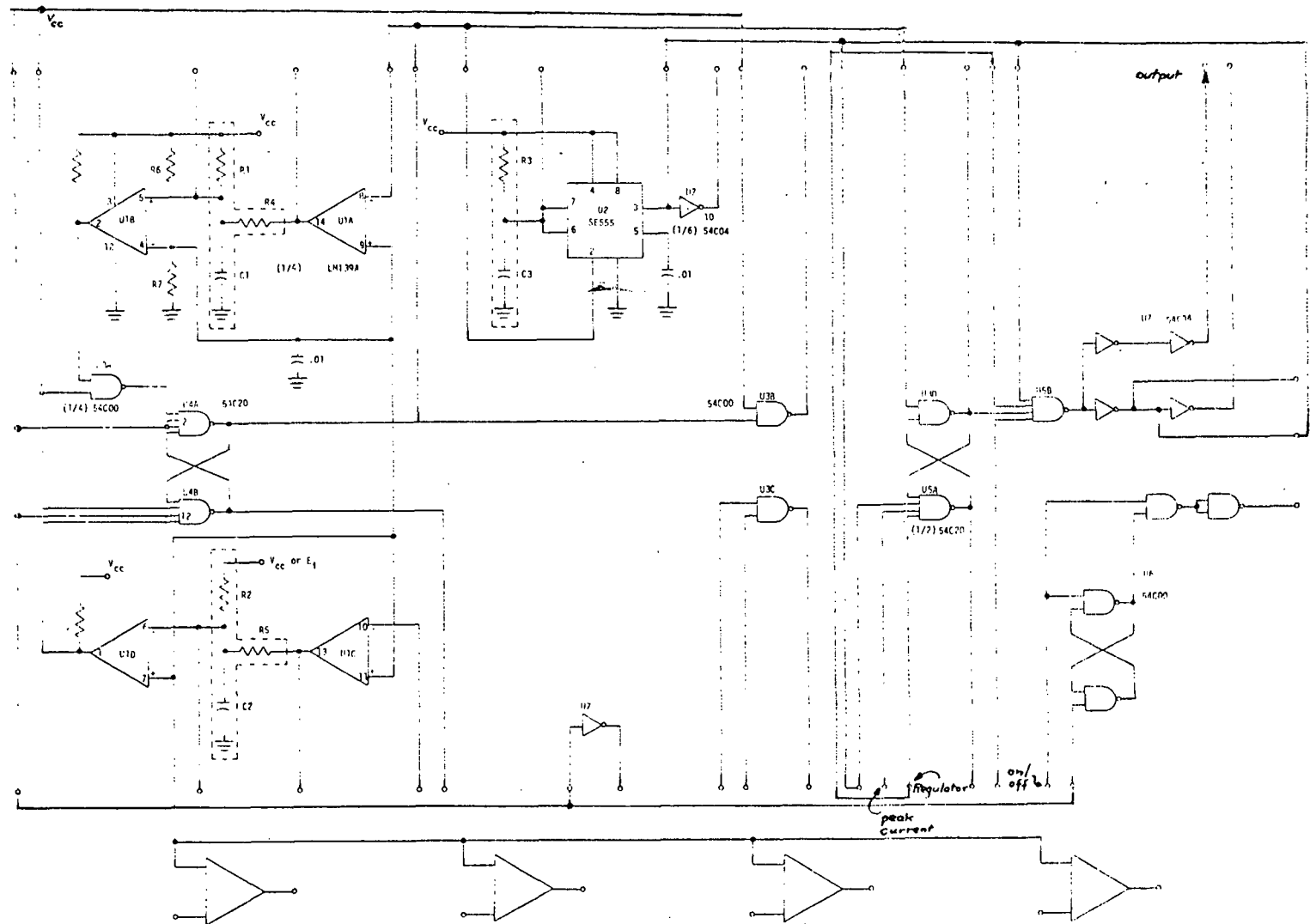


FIGURE 15(B) SCHEMATIC DIAGRAM OF A CONSTANT-FREQUENCY DIGITAL SIGNAL PROCESSOR

	<u>HTL</u>	<u>TTL</u>	<u>CMOS</u>
Parts Count	Low*	High	High
Noise Immunity	Excellent	Low	Good
Power Loss	High	Low	Negligible
Requirement for Supply Regulation	Need less regulation	Needs good regulation	Needs least regulation
Propagation Delay	Slow**	Fast	Fastest

Primarily due to its negligible loss, the CMOS gates were chosen for deliverable breadboards. However, all three types of logics were demonstrated to be adequate for DSP applications. As a matter of fact, by lowering the logic supply voltage from the present 10V to 5V, all CMOS IC's in deliverable breadboards can be readily replaced by their TTL equivalents without affecting dc-dc converter operations.

5.3.3 Summary Remarks on the Common Schematics

Through different connections of component parts within a common DSP schematic diagram, different DSP's executing various duty-cycle control modes can be implemented using any type of digital IC's. The commonality is made possible primarily by having the same components performing different functions in different DSP's. Regardless the DSP configuration, regulation, command, and protection signals are processed, from which a proper digital signal is generated at the DSP output to provide a predictable control of the power switch and therefore an orderly converter operation during steady-state and transient conditions. In addition, the DSP enables an user to readily control the design of the operating frequency for all

*Low HTL parts count due to the availability of HTL pulse stretcher and the ability to use HTL NAND's as threshold detectors due to zener references that are contained within the HTL NAND's.

**Slow yet adequate for regulator application.

types of switching regulators through the adjustment of the RC time constants without the need for any magnetic timing element. These features, along with the circuit simplicity and low loss ($< 50\text{mW}$), has complemented the high-performance Analog Digital Processor (discussed in Section 4) to greatly enhance the utility of the SCM.

5.4 SCHEMATIC OF DSP CONTROLLING PUSH-PULL TYPE OF POWER CONVERTERS

Discussed in the previous section was the common schematic diagram for DSP's controlling single-ended power converters. While single-ended converters represent a major portion of practical designs, there are other converter types employing two power switches in a phase-complementary manner for input- and output-filter size and weight savings. Examples of these converters include pulse-width modulated parallel inverter and two phase-displaced single-ended power configurations sharing a common output-filter capacitor. The difference between the two-channel and the single-ended DSP is that the two-channel DSP must now process the same digital input signals to effect a proper duty cycle control for two power switches instead of a single switch. The functional block diagram and the detailed implementation are fairly similar other than differences resulting from the need for controlling two switches versus one.

One of deliverable power converter breadboards is a pulse-modulated parallel inverter. The duty-cycle control used for the two power switches is based on constant- $E_i T_n$. The basic schematic diagram of the constant- $E_i T_n$ DSP is shown in Figure 16. Due to the need for an on-time interval and a minimum off time interval for each of the two power switches, the front end of the DSP where T_n and T_m are configured is different from that of a single-ended DSP shown in Figure 15. Similarly, due to the need for two DSP digital outputs instead of one, the power interface portion now demands one more NAND. Other than these differences and their attendant connection changes, the DSP's shown in Figures 15 and 16 contain identical basic functions.

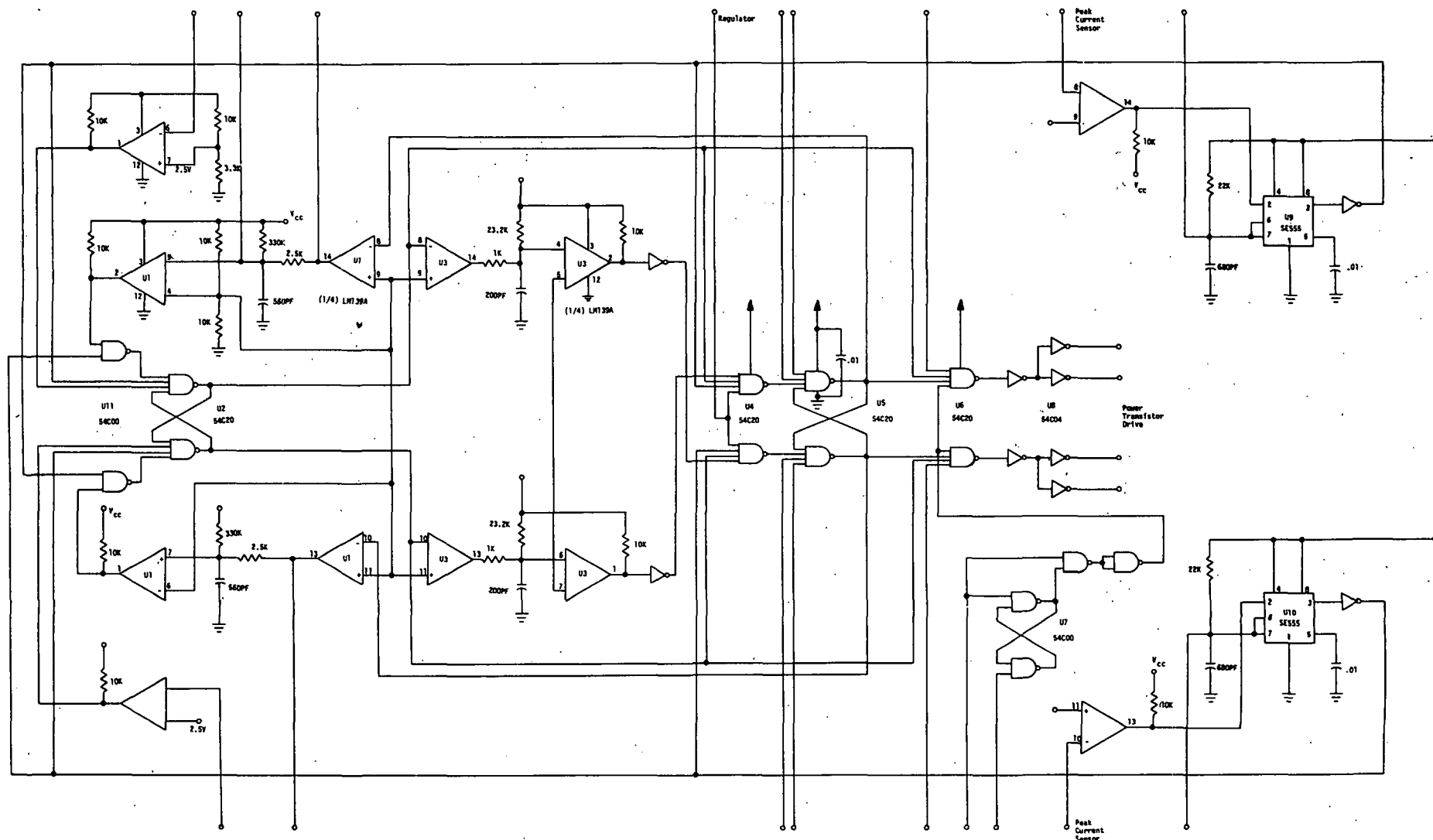


FIGURE 16 A TWO-CHANNEL CONSTANT- $E_i T_n$ DIGITAL SIGNAL PROCESSOR

6. SCM DEMONSTRATION BREADBOARDS

Having described the SCM, ASP, DSP, and their merits, this section shows typical performance results that can be obtained from different types of power converters using the SCM control. Following the description of demonstration converter types, other essentials of the SCM control will be presented. Steady-state performance characteristics will be summarized for these converters. More importantly, transient regulation and protection performance features will be emphasized through actual testing under large-disturbance conditions. Finally, the SCM submodule division and interchangeability will be discussed.

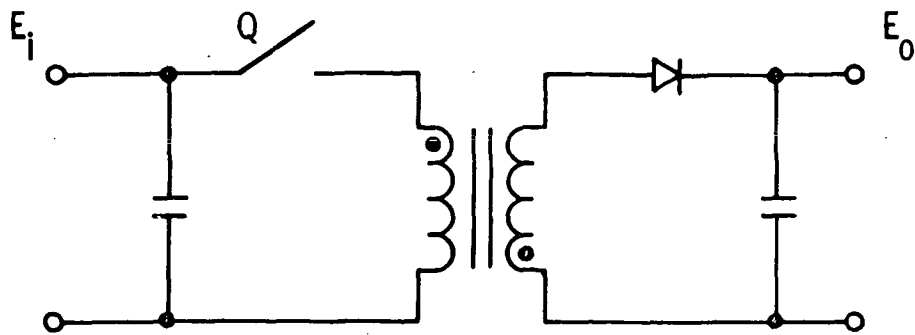
6.1 DEMONSTRATION BREADBOARD POWER CONVERTER TYPES

The program provided for the demonstration of SCM on three most commonly used dc to dc converter configurations. Shown in Figure 17, these configurations are: (1) the buck boost converter, (2) the series-switching buck converter, and (3) the pulse-modulated parallel-inverter converter. The operation of these converters is described in Appendix A.

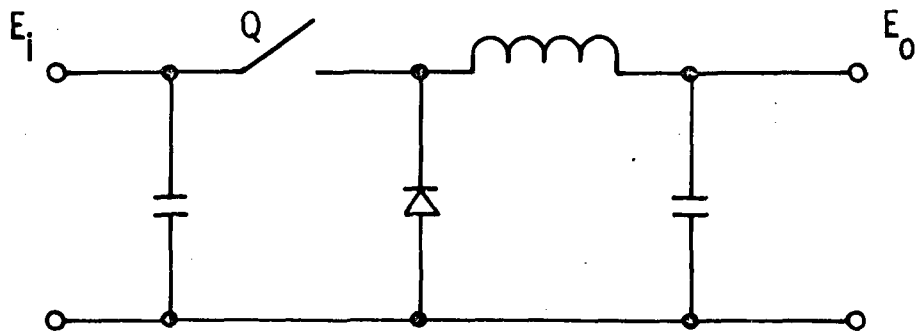
6.2 THE BASIC SCM SCHEMATIC DIAGRAM

While the most fundamental SCM blocks, the ASP and the DSP, have been discussed in details, two other supporting circuitries are essential to the well-being of the SCM in terms of its operation and its universality. These circuitries include the SCM logic power supply and the external ramp generator needed for maintaining stable constant-frequency operation when the operating duty cycle exceeds the 50% stability limit. Principle of the stabilizing ramp has been presented previously in Section 4.6.3.2.

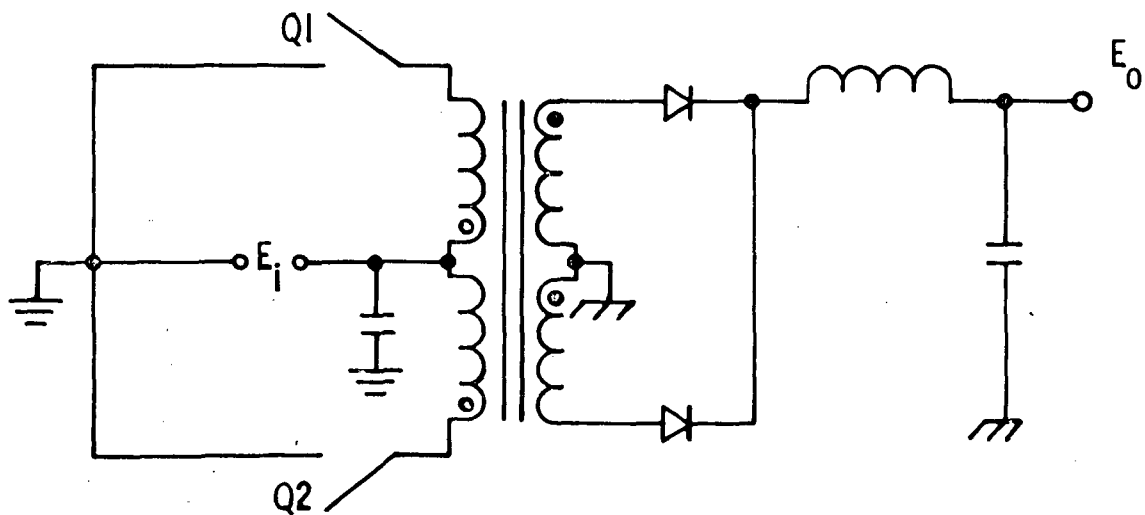
Together with these supports, the complete SCM schematic containing all SCM essentials is given in Figure 18. In conjunction with the details provided previously for ASP and DSP, the following clarifications serve to describe the SCM as a complete control entity:



(A) Buck-Boost Converter



(B) Series-Switching Buck Regulator



(C) Pulse-Modulated Parallel Inverter Converter

FIGURE 17 POWER CONFIGURATIONS OF THE THREE DEMONSTRATION CONVERTERS

- (1) The logic power supply is a conventional low-power "ripple" regulator receiving power from the converter input and delivering an adjustable regulated output between 5V and 12V. A zener diode is used to clamp the regulator IC so that the converter input can be higher than the IC voltage rating (40V for $\mu A723$). A winding on the "ripple" regulator choke is grounded at the output return, which supplies a closely regulated voltage to the ASP whose ground is at the output return due to its necessity of sensing the output voltage for regulation control. Thus the ASP is provided with a bias supply without destroying the control-circuit input/output isolation. The constant presence of this voltage under all dynamic conditions (e.g., converter starting or sudden output short circuit) releases the ASP operational amplifier from any erratic behavior that might be caused by an insufficient bias supply, thus enhancing a predictable control throughout all line/load transients. Such a complete control is, of course, a basic objective of the SCM.
- (2) An ASP is shown in Figure 18 to sense and regulate the output voltage. A similar circuit can be used in addition for sensing and regulating output current. In fact, such an additional ASP is used in the deliverable breadboards.
- (3) As demonstrated in Section 4.6.3.2, the constant-frequency stabilization ramp must be added during the on time when a clock is used to initiate the on time. The generation of such a ramp is shown in Figure 18. Transistor Q3 across C10 conducts during T_f and blocks during T_n . The ramp is produced by the charging of C10 through R10 during T_n .

The ramp is enhanced as a voltage source by unity-gain amplifier U12. With its dc component blocked by C11, the ac ramp component is impressed across the primary of T1, and the secondary output with the proper phasing is inserted in series with the output of the ASP integrator-amplifier to produce the required ramp.

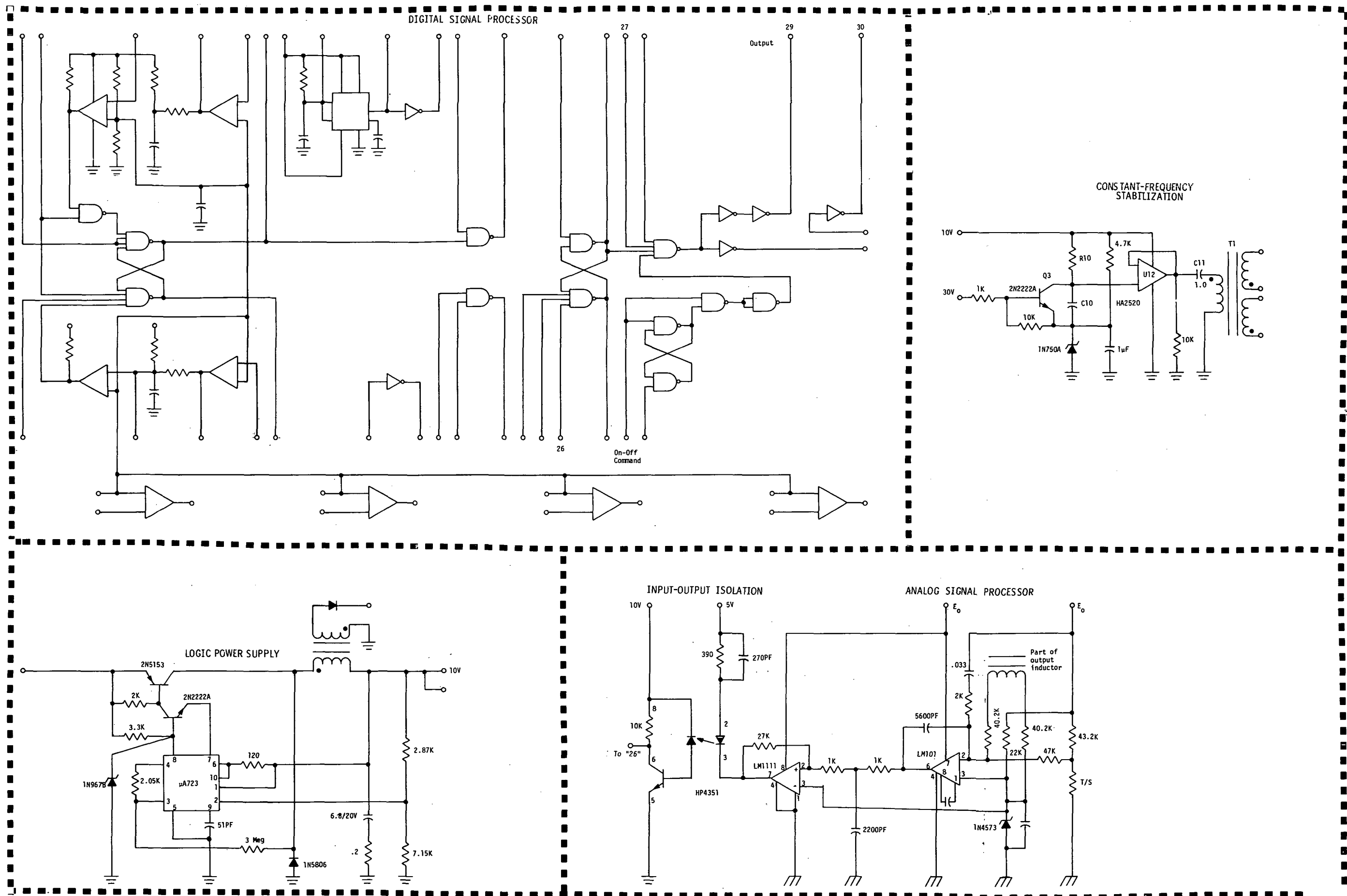


FIGURE 18 BASIC ESSENTIALS OF THE SCM CONTROL SYSTEM

- (4) While the ramp indeed extends the stable duty cycle beyond the 50% limit, its attendant effect is the reduction of the gain of the pulse modulation stage. The higher the ramp slope, the less is the gain. Consequently, the use of an excessive ramp slope is neither required from a stability viewpoint, nor is it recommended from the transient-response consideration. For a given application with a specified input voltage range, the need for higher ramp slope invariably occurs at the low line as such is the case for the high duty cycle. Consequently, an ideal external ramp is one that will have the highest slope at low line, and the slope diminishes with the line-voltage increase until it disappears when the required duty cycle for regulation is below 0.5. A ramp of this character can be approximated by supplying $R_{10}C_{10}$ from a voltage source that decreases as the converter input voltage increases. Such a source was indeed implemented in the deliverable breadboards strictly for demonstration purpose. However, the extra parts count required for the implementation (ten parts) is hardly justified in view of the limited transient-response improvements gained.

In summary, two SCM subcircuits, one a current-regulating ASP, the other a variable voltage source for optimum ramp formation, are included in the deliverable breadboards. Since they are not regarded as the essential ingredients of the SCM control system, they are not included in the basic SCM schematic shown in Figure 18. However, they are included in the deliverable converter breadboards, to be presented in the next section.

6.3 SCHEMATIC DIAGRAMS FOR DELIVERABLE CONVERTERS

The power circuits for all three converters were developed in Contract NAS 3-18918. The schematics and component values were presented in detail in reference [3]. The control circuit schematics and component values have been given in Figures 15, 16, and 18 of this report.

Key design requirements for all three converters are presented in Appendix B.

6.4 DEMONSTRATION BREADBOARD STEADY-STATE PERFORMANCE

Steady-state performance data taken on three types of converter breadboards over the following line, load, and temperature ranges have shown the converter capabilities either meet or exceed the specification requirements given previously in Appendix A.

<u>Converter</u>	<u>Input Voltage (V)</u>	<u>Output Load (W)</u>	<u>Temperature (°C)</u>
Buck Boost	20 to 40	4.2 to 42	-25 to +85
Series Buck	24 to 40	4 to 40	-25 to +85
Parallel Inverter	24 to 40	30 to 40 (+1kV) 3.75 to 7.5 (+15V) 3.75 to 7.5 (-15V) 2.5 to 5.0 (+5V)	-25 to +85

Under these test conditions, the steady-state performance data are presented in detail in the Final Test Report submitted to NASA. A brief summary of test data is given in Table 1.

6.5 DEMONSTRATION BREADBOARD TRANSIENT PERFORMANCE

The converter transient response is important with regard to the following power system performance aspects:

- (1) During severe line and load transients such as converter starting and excessive transient output faults, the electrical stresses on all power-handling components of the converter must be controlled to within their safe operating limits. If this control is not established, the converter reliability would suffer, and the all-important reliability assessment based on the collective statistical failure rate of individual component would be of little real value.
- (2) Instrumentation and equipment loads often require a power quality which stays within a given specification during not only steady-state, but also transient line and load operations. This specification is generally in common with the converter output regulation or peak-peak ripple requirement, whichever is greater.

TABLE 1 SUMMARY OF SCM DEMONSTRATION BREADBOARD CONVERTER TEST RESULTS

PERFORMANCE PARAMETERS	BUCK BOOST		SERIES SWITCHING		PARALLEL INVERTER
	Const. $E_i T_n$	Const. Freq.	Const. $E_i T_n$	Const. Freq.	Const. Freq.
** Worst Audio plus switching ripple as a percentage of output voltage (+)	0.34% at 400Hz	0.32% at 800Hz	0.33% at 1kHz	0.33% at 1kHz	0.2% at 1.6kHz
*** Worst-case source EMI, all meet MIL-STD-461, Notice 3	25mA at 6.3kHz	5mA at 27.2kHz	35mA at 5kHz	3mA at 25kHz	7mA at 24kHz
Full Load Efficiency, at room temperature	90.5% at $E_i = 30V$	90.2% at $E_i = 30V$	92.4% at $E_i = 32V$	92.0% at $E_i = 32V$	85.4% at $E_i = 32V$
DC Output Voltage regulation (+)	0.038%	0.034%	0.09%	0.05%	0.11%
Output Current Regulation (+)	← Less than $\pm 5\%$ at 120% full level →				Overload shutoff
** Worst-case output impedance at full load	0.2 Ω	0.2 Ω	0.19 Ω	0.21 Ω	1kV

* The power circuit of the parallel inverter uses a particular two-core transformer adaptable to constant- $E_i T_n$ control only.

** The frequency listed is the audio disturbance frequency at which worst attenuation occurs. The amplitude of the audio input is 2.8V RMS (8V peak-to-peak). The worst output response is within the 1% ripple specification.

*** The frequency listed is the switching frequency of the converter. The 5 and 6.3kHz occur at light-load conditions for the respective converters when output filter inductor currents are discontinuous.

** The frequency listed is the load-current disturbance frequency at which worst output impedance occurs.

In relation to these desirable performance aspects, oscillograms of waveforms were taken on all three converters under large line and load changes. The waveforms included the line/load step change, the power-switch current, and/or the output voltage under the following transient operations:

- Transient output voltage response to a step input voltage change.
- Transient output voltage response to a step load change.
- Power switch current and converter output voltage following a sudden output short circuit.
- Power switch current and converter output voltage following a converter command-on, with peak-current protection in effect. Converter output is set at full load.
- Same as above, with peak-current protection disabled.
- Power switch current and converter output voltage following a converter command-on, with peak-current protection in effect. Converter output is set at no load.
- Same as above, with peak-current protection disabled.

The waveforms are obtained for all converters operating in constant- $E_i T_n$ and constant-frequency duty-cycle control when such controls are applicable. Only constant- $E_i T_n$ control is applied to the parallel-inverter converter, as this is the only control adoptable to the two-core-transformer power configuration used in the power-circuit design. The oscillograms are shown in Figures 19 to 25, from which the following SCM transient performances can be established.

- (1) The current level in the power switch (and therefore of all power components) during any severe line and load transients was limited to within 140% of the respective maximum steady-state value. The control was accomplished through the design of peak-current protection and the DSP.

- (2) The design goal of meeting the 1% steady-state ripple specification was achieved for large step line and load changes. All transients were critically damped, indicating good dynamic stability. No output-voltage overshoot was observed during starting. These characteristics were made possible by the ASP design.

Many interesting observations can be made on the oscillograms from Figures 19 to 25. A complete identification on the nature of each waveform in its minute detail is not the primary objective here. However, the following points of significance can be noted for the respective figures:

Figure 19. Transients During A Step Input Voltage Change

- The output voltage excursion for the three converters are, from the top, less than 100mV, 100mV, and 6000mV, respectively. Corresponding to the regulated output voltage of 28V, 20V, and 1000V, the excursions are within the 1% ripple specification (280mV, 200mV, and 10V, respectively) for the three converters.
- No disorderly current can be observed during the input-voltage transition.

Figure 20. Transients During A Step Load Change

- The output voltage excursion for the three converters are, from the top, less than 100mV, 150mV, and 4000mV, respectively. Corresponding to the regulated output voltage of 28V, 20V, and 1000V, the excursions are within the 1% ripple specification for the three converters.
- The absence of any prolonged oscillation is in good agreement with the absence of any peak in output-impedance measurement over the frequency spectrum.

Figure 21. Transients During A Sudden Output Short Circuit

- The pictures were taken with the current regulator disabled to show the effective protection offered by the peak-current sensor alone.
- The power-switch current is limited to about 140% of the maximum nominal steady-state peak current. The current level is therefore precisely controlled.
- There is no output voltage overshoot during recovery from output short for the first two converters. For the parallel-inverter converter, the design is such that upon an output short the converter is turned off. A similar oscillogram to those of the first two converters is thus not applicable.

- For the parallel inverter, the OL protection circuit latches the converter off 90ms after the short is applied. During this time, power switch current is limited to about 140% of the nominal peak current.

Figure 22. Converter Command-On at Full Load, with Peak Current Protection in Effect

- Current regulators are disabled to demonstrate the protection of the peak current sensor alone.
- There is no output-voltage overshoot during converter start-up.
- There is no erratic current during converter start-up. The current is limited to 6A, 4A, and 12A, respectively for the three converters by the peak-current protection.

Figure 23. Converter Command-On at Full Load, with Peak Current Protection Disabled

- Current regulators are disabled to demonstrate what can happen to power-switch currents during command-on without peak-current protection.
- For the three converters, the initial switching currents were erratic, and reached 40A, 15A, and 25A, respectively. Compare these pictures with those of the previous page when a peak-current sensor was provided, the effectiveness of the peak-current protection is clearly demonstrated.

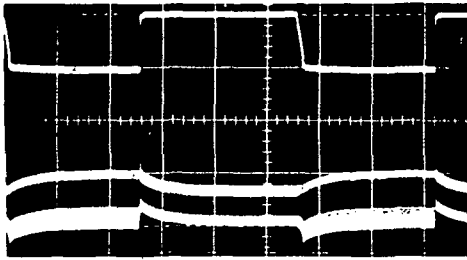
Figure 24. Converter Command-On at No Load, with Peak Current Protection In Effect

- Same comments in Figure 23 applicable.
- The test is not applicable to parallel-inverter converter, as it does not accommodate the open-load operation.
- For the other two converters, the power switch current is clearly triangular at light load, i.e., each cycle the power switch starts with zero current.

Figure 25. Converter Command-On at No Load, with Peak Current Protection Disabled

- Same comments in Figure 24 applicable.
- Comparing Figure 25 with Figure 24 reveals vividly the utility of the peak-current protection.

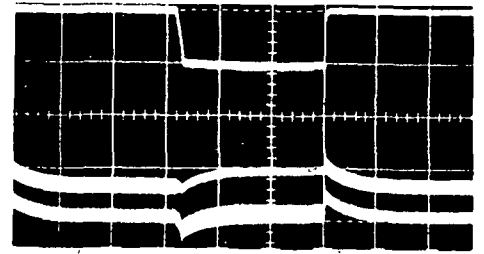
BUCK
BOOST
CONV.



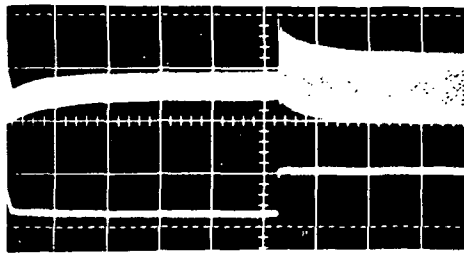
INPUT VOLTAGE
20V/DIV.

TIME : 20ms/DIV

OUTPUT VOLTAGE
0.2V/DIV



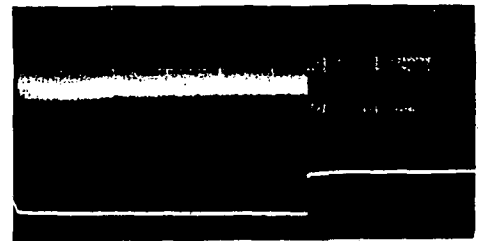
SERIES
BUCK
CONV.



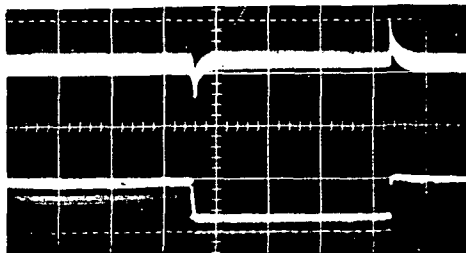
OUTPUT VOLTAGE
0.1V/DIV.

TIME: 5ms/DIV

INPUT VOLTAGE
20V/DIV



PARALLEL
INVERTER
CONV.



OUTPUT VOLTAGE
10V/DIV

TIME: 20ms/DIV

INPUT VOLTAGE
20V/DIV

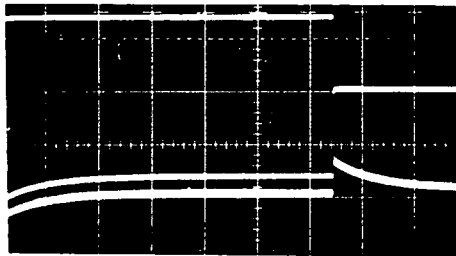
NA

CONSTANT- $E_i T_n$

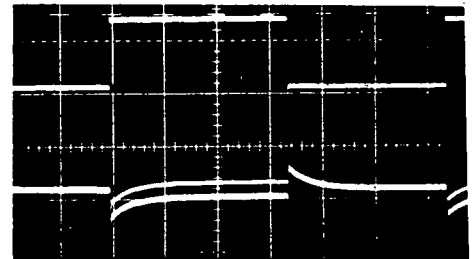
CONSTANT-FREQUENCY

FIGURE 19. TRANSIENT OUTPUT VOLTAGE RESPONSE TO A STEP INPUT VOLTAGE
CHANGE INPUT: BETWEEN 24V AND 40V

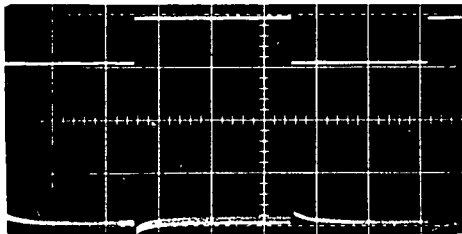
BUCK
BOOST
CONV.



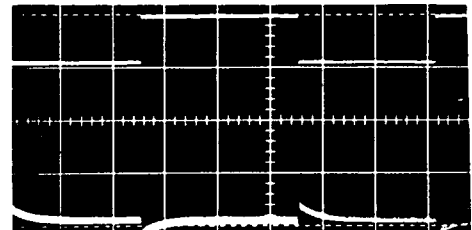
OUTPUT CURRENT
1A/DIV.
TIME : 20 ms/DIV.
OUTPUT VOLTAGE
0.5V/DIV.



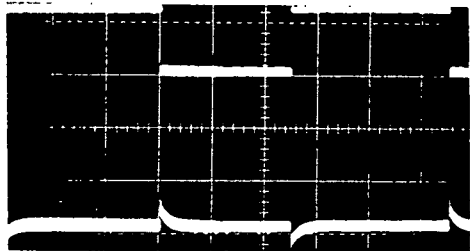
SERIES
BUCK
CONV.



OUTPUT CURRENT
2A/DIV
TIME: 20ms/DIV
OUTPUT VOLTAGE
0.5V/DIV



PARALLEL
INVERTER
CONV.



OUTPUT CURRENT
5mA/DIV
TIME: 10ms/DIV
OUTPUT VOLTAGE
10V/DIV

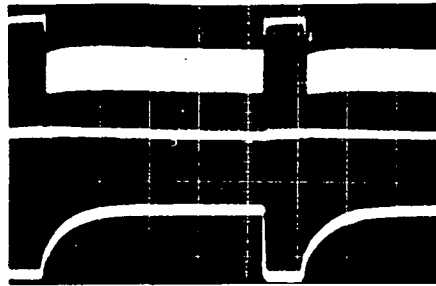
NA

CONSTANT- $E_i T_n$

CONSTANT-FREQUENCY

FIGURE 20. TRANSIENT OUTPUT VOLTAGE RESPONSE TO A STEP LOAD CHANGE
LOAD: BETWEEN 10% AND 100% FULL LOAD

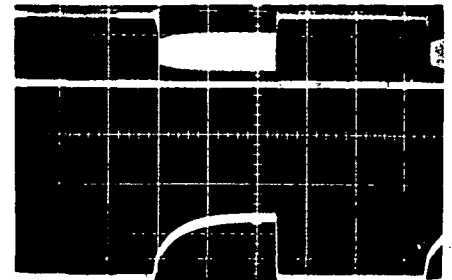
BUCK
BOOST
CONV.



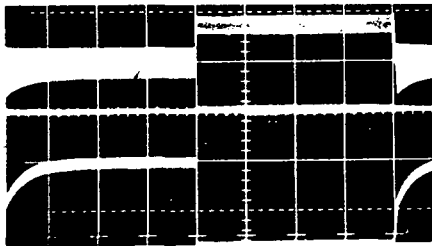
POWER SWITCH CURRENT
2A/DIV.

TIME : 20 ms/DIV.

OUTPUT VOLTAGE
20V/DIV.



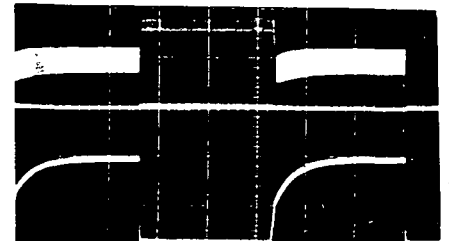
SERIES
BUCK
CONV.



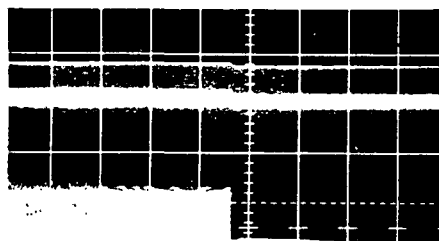
POWER SWITCH CURRENT
2A/DIV.

TIME: 20ms/DIV

OUTPUT VOLTAGE
10V/DIV



PARALLEL
INVERTER
CONV.



OUTPUT VOLTAGE
5V/DIV

TIME: 20ms/DIV

POWER SWITCH CURRENT
10A/DIV

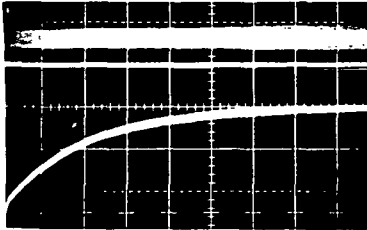
NA

CONSTANT- $E_i T_n$

CONSTANT-FREQUENCY

FIGURE 21. POWER SWITCH CURRENT AND CONVERTER OUTPUT VOLTAGE DURING REPETITIVE OUTPUT SHORT CIRCUIT

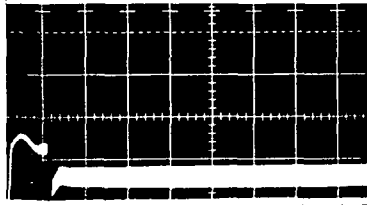
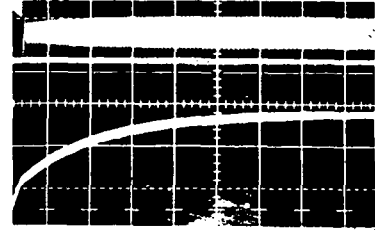
BUCK
BOOST
CONV.



POWER SWITCH CURRENT
4A/DIV.

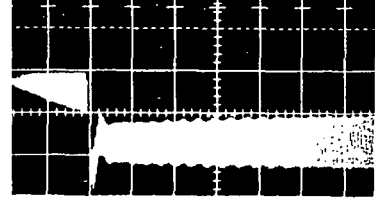
TIME : 5 ms/DIV.

OUTPUT VOLTAGE
10V/DIV.

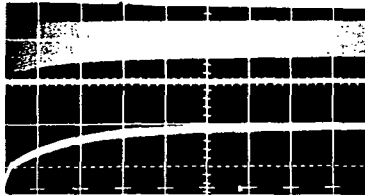


EXPANDED VIEW OF
POWER SWITCH CURRENT
4A/DIV. (CONST. VOLT-SEC)
2A/DIV. (CONST. FREQ.)

TIME : 1 ms/DIV.



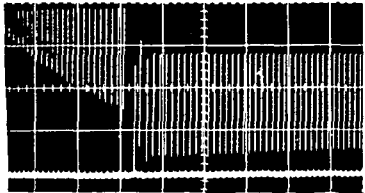
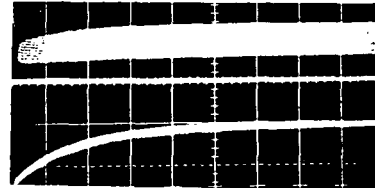
SERIES
BUCK
CONV.



POWER SWITCH CURRENT
2A/DIV

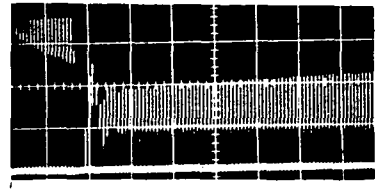
TIME: 5ms/DIV

OUTPUT VOLTAGE
10V/DIV

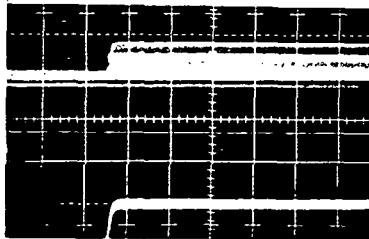


EXPANDED VIEW OF
POWER SWITCH CURRENT
1A/DIV

TIME: 0.5ms/DIV



PARALLEL
INVERTER
CONV.



POWER SWITCH CURRENT
10A/DIV

TIME: 50ms/DIV

OUTPUT VOLTAGE
1KV/DIV

NA

CONSTANT- $E_1 T_n$

CONSTANT-FREQUENCY

FIGURE 22. POWER SWITCH AND OUTPUT VOLTAGE FOLLOWING CONVERTER COMMAND-ON
WITH FULL LOAD INPUT VOLTAGE: 40V

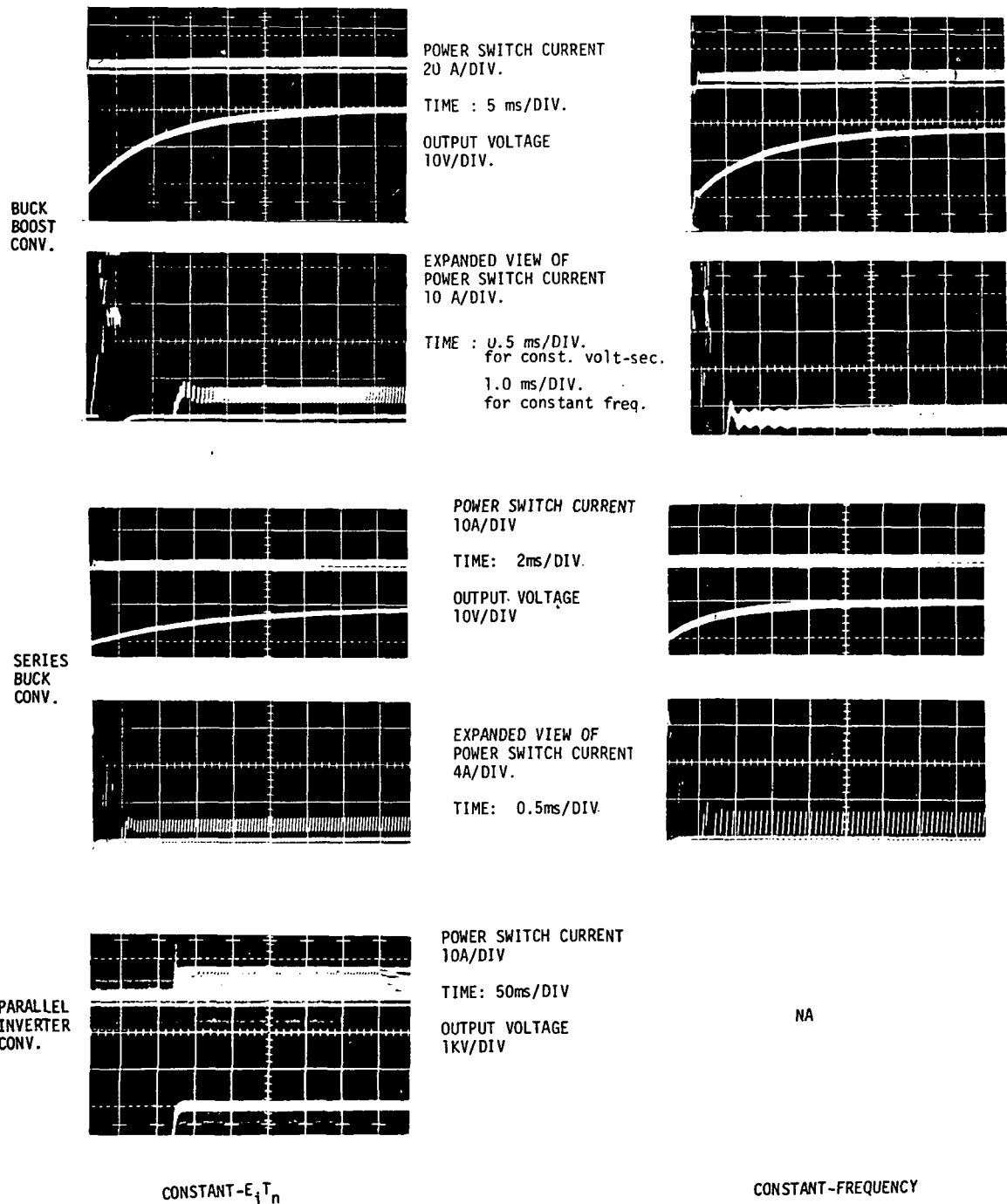
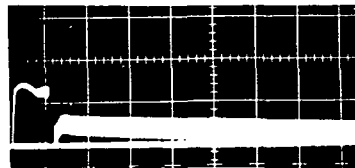
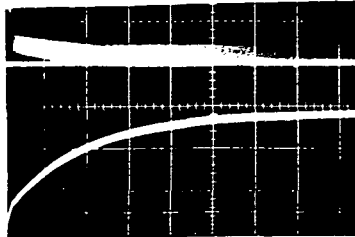


FIGURE 23. POWER SWITCH CURRENT AND CONVERTER OUTPUT VOLTAGE FOLLOWING CONVERTER COMMAND-ON WITH FULL LOAD AND WITH PEAK-CURRENT PROTECTION DISABLED, INPUT VOLTAGE: 40V

BUCK
BOOST
CONV.



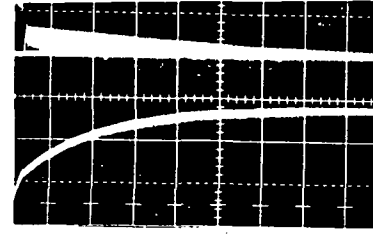
POWER SWITCH CURRENT
4A/DIV.

TIME : 5ms/DIV.

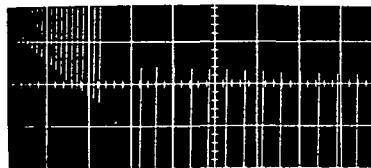
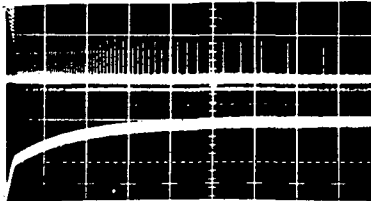
OUTPUT VOLTAGE
10V/DIV.

EXPANDED VIEW OF
POWER SWITCH CURRENT
4A/DIV.

TIME : 1ms/DIV.



SERIES
BUCK
CONV.



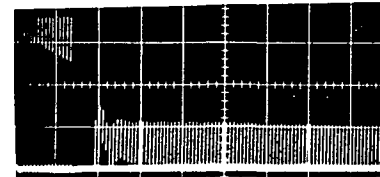
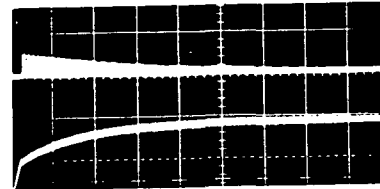
POWER SWITCH CURRENT
2A/DIV

TIME: 5ms/DIV

OUTPUT VOLTAGE
10V/DIV

EXPANDED VIEW OF
POWER SWITCH CURRENT
1A/DIV

TIME: 0.5ms/DIV

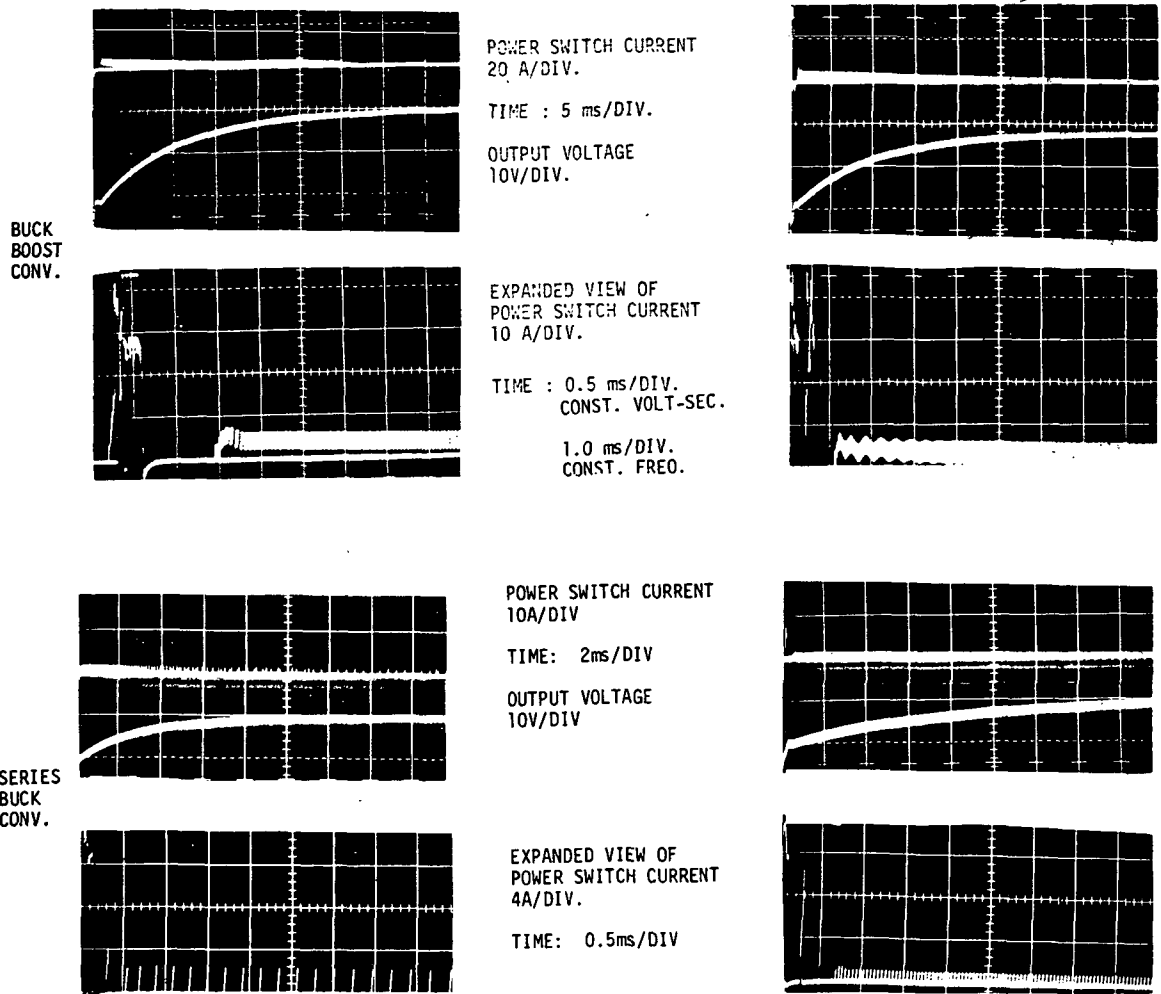


THE PARALLEL-INVERTER CONVERTER IS NOT APPLICABLE
FOR NO-LOAD OPERATION

CONSTANT- $E_i T_n$

CONSTANT-FREQUENCY

FIGURE 24. POWER SWITCH CURRENT AND CONVERTER OUTPUT VOLTAGE FOLLOWING
CONVERTER COMMAND-ON WITH NO LOAD. INPUT VOLTAGE: 40V



THE PARALLEL-INVERTER CONVERTER IS NOT APPLICABLE
FOR NO-LOAD OPERATION

CONSTANT- $E_i T_n$

CONSTANT-FREQUENCY

FIGURE 25. POWER SWITCH CURRENT AND CONVERTER OUTPUT VOLTAGE FOLLOWING
CONVERTER COMMAND-ON WITH NO LOAD AND WITH PEAK-CURRENT
PROTECTION DISABLED. INPUT VOLTAGE: 40V

6.6 SCM SUBMODULE DIVISION AND INTERCHANGEABILITY

Shown in Figure 26 are three power-converter breadboards. They are the buck boost converter at the upper left, the series buck converter at the upper right, and the parallel-inverter converter at the lower center. The power circuit of each converter occupies the upper portion of each breadboard. The SCM used to control the power circuit are separated into: (1) the basic control module, and (2) different duty-cycle submodules.

6.6.1 The Basic Control Module

The basic control module occupies the lower left block in each breadboard. It contains the voltage and current ASP's, the DSP with the exception of the RC's needed for frequency adjustment, and the logic power supply. The basic control module for the buck boost converter is identical to that of the series buck converter. While the functions of the basic control module remain unchanged for the parallel inverter when compared with the other two converters, the fact that it controls two power switches instead of one explains its apparent increase in complexity.

6.6.2 Duty-Cycle Control Submodules

Two duty-cycle control submodules are fabricated for each of the buck-boost and series buck converters. The submodule located in the lower center of each breadboard contains the various adjustable RC time constants needed in the constant- $E_i T_n$ (or constant- T_n) control. The submodule located on the right side of each breadboard contains the various adjustable RC's and the external ramp needed in the constant-frequency control. The inclusion of the ramp generation is responsible for the higher complexity of the constant-frequency submodule.

Electrical connections between the respective submodules and the rest of the converter are carefully designed so that a change between the two different duty-cycle operations is made simply by unplugging one submodule and connecting the other. There is no need for any rewiring or soldering in carrying out a change between the two duty-cycle control modes.

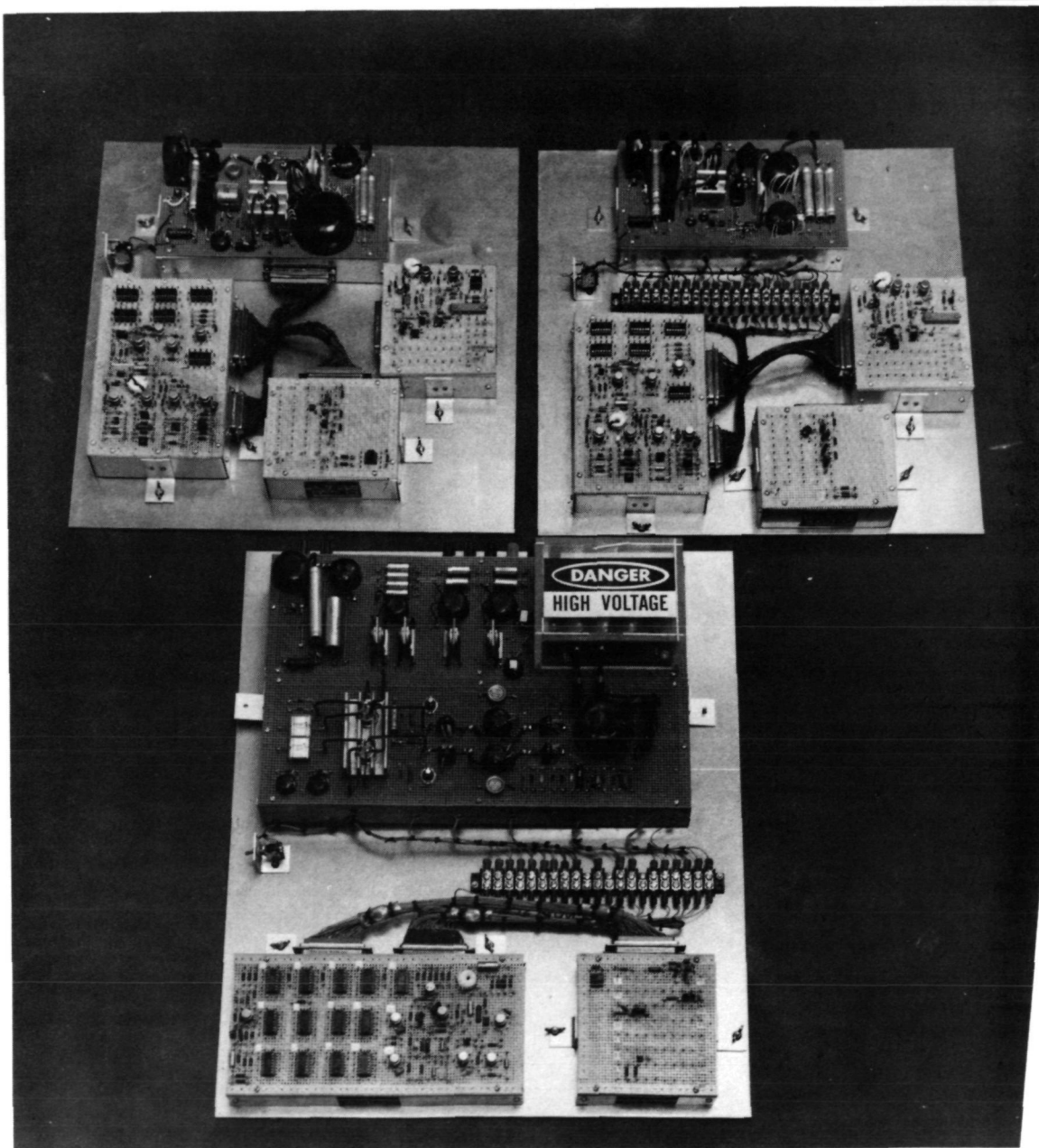


FIGURE 26. THREE DELIVERABLE CONVERTER BREADBOARD

Needless to say, the provision of these two submodules and their respective separation with the basic control module are motivated entirely by the program objective of readily demonstrating different duty-cycle control modes. In practical applications where only one duty cycle control mode is all a converter needs, the corresponding submodule can be combined into the basic control module to form a single SCM control board, thus providing a much less complicated outlook for the SCM.

As previously stated, the two-core transformer used in the parallel-inverter converter is inherently a constant- $E_i T_n$ design. Consequently, only the constant- $E_i T_n$ submodule is provided in the converter breadboard.

6.6.3 Interchangeability of the Basic Control Module

Since the basic control modules for the buck-boost and series-buck converters are identical, they are obviously interchangeable within the two converters for any duty-cycle control mode. This fact was experimentally demonstrated in the deliverable converter breadboards.

In addition, each corresponding submodule in the two converters contains essentially the same components. The only reason they are not interchangeable is because the adjustable RC time constants are not the same, as the power circuits were not designed to operate at the same frequency or require the same external ramp. However, the switching frequency and the ramp can be standardized as well if a family of standardized power-circuit designs were to emerge in the future. When that happens, there is no reason why the entire SCM control board cannot be made interchangeable.

7. SCM MODELING AND ANALYSIS

Power processing technology has, from necessity, been a rapidly evolving technology. However, perhaps due to the preoccupation of making products on schedule and within budget, the effort associated with switching-regulator modeling and analysis has been unable to keep pace with the degree of sophistication already achieved in circuit developments. The SCM design has more or less followed this pattern; SCM-controlled high-performance regulators using a variety of duty-cycle control modes were developed prior to any serious SCM modeling and analysis attempt. With the capability of SCM now well established, an analytical program to achieve a comprehensive understanding of the SCM control for different switching regulators is in order.

Considering carefully the basic objective of SCM modeling and analysis and the limited program resources, the following decisions were made during the program:

- (1) The modeling and analysis will center on the local stability of the SCM-controlled regulator, as the stability is often the utmost concern in designing the control circuit of a switching regulator. Since one of the demonstrated SCM merits is that the SCM-controlled regulator stability is relatively immune to output filter parameter changes, a stability analysis would provide the needed theoretical substantiation. To be readily comprehensible by most regulator designers, the analysis is preferably carried out in the frequency domain using S-transform. Despite the diminishing accuracy of this analytical approach with a higher signal to switching frequency ratio, its use here is made palatable by the fact that the output filter frequency at which the autocompensation occurs is significantly lower than the switching frequency.
- (2) The powerful tool of modern control theory and digital-computation techniques should also be exploited to accurately model the non-linear, discrete nature of a dc to dc switching regulator. The effort, based on exact state-space representation, will enhance a unified description of all types of switching regulators using any duty cycle control mode.
- (3) The byproduct of the time-domain state-space approach should be a cost-effective computer simulation program actually portraying the duty-cycle switching and regulator behavior under large-signal disturbances. Aided by time-domain modeling, the simulation should be less time-consuming than other general-purpose tools such as ECAP, SCEPTRE, or CSMP.

In the following sections, frequency-domain stability analysis will be presented first. The philosophy of a generalized time-domain analysis is then outlined, from which the analysis is performed for constant- T_n and constant-frequency duty-cycle control modes using the series buck regulator for illustration. A cost-effective digital simulation program based on time-domain modeling is also included.

7.1 SCM-CONTROLLED REGULATOR FREQUENCY-DOMAIN STABILITY ANALYSIS

The most often used frequency-domain stability representation is through Bode plot of the open-loop transfer function. In a conventional single-loop system, the transfer function is the same regardless of the location at which the analyst chooses to mentally or physically open the loop. This freedom no longer holds for the multiple-loop SCM. Opening the loop at different locations in relation to different loops generally calls for different interpretation of analytical results. It is not unusual for a multiple-loop design to exhibit essentially a -6db/octave slope with a phase margin of 90° when the open-loop transfer function is analyzed at a certain location, while concurrently the transfer function viewing from another location would suggest an excessive phase shift. In assessing the stability of a SCM-controlled power processor through the system open-loop transfer function, one must therefore be careful in the selection and the interpretation of the loop opening.

7.1.1 A SCM-Controlled Power Processor

A SCM-controlled power processor is shown in Figure 27, using a buck switching regulator as an example. The reason for choosing the buck regulator is for clarity. Since the primary objective here is to identify the autocompensation nature of the SCM, the regulator serves the purpose with the least analytical complication, as its equivalent output filter are known to be independent of the operating duty cycle [21].

Input voltage E_i , power switch Q , diode D , inductor L with winding resistance R_L , capacitor C with inherent resistance R_C , and load R_O , constitute the basic buck switching regulator.

Starting from point A at the tip of diode D and tracing clockwise, the ac voltage across L and the dc voltage across R are separately sensed to become actuating signals for two closed loops identified in Figure 27 as Loops II and I. For discussion purpose, a constant- T_n control is assumed.

Loop I senses the average load voltage, the signal is divided down by resistors R1-R2. Through a gain adjusting resistor R3, the output of the divider is fed to the "inverting" terminal of the integrator-amplifier. The amplifier is assumed to have a large dc gain K.

Loop II senses the instantaneous ac voltage across the inductor. Through a gain-adjusting resistor R4, the signal is fed differentially into the "inverting" and the "non-inverting" integrator terminals. The algebraic sum of this ac signal and the dc output signal from the voltage divider is compared to reference E_R , the error is integrated by the integrator-amplifier, where C_1 is the feedback capacitor of the integrator.

Loop III containing lead network C_2R_5 is used to improve the output dynamic performance of the power processor.

The phase of the ac inductor voltage in relation to the integrator terminals is such that a ramp voltage with a positive (negative) slope exists during the off (on) time of power switch Q. For the purpose of this analysis, the duty-cycle control implemented in the Digital Signal Processor of Figure 27 is assumed to be constant $E_i T_n$, i.e., the on time T_n is inversely proportional to the input voltage E_i . When the instantaneous value of the ramp at point B of Figure 27 reaches threshold level E_T of the threshold detector, the pulse output from the detector will actuate the DSP. The DSP turns on switch Q for a predetermined time interval T_n , during which the slope of the integrator output ramp, is negative. The termination of T_n (including the power switch storage time) brings instant polarity reversal on the voltage across inductor L. The integrator output ramp thus reverts to a positive slope. The instant the ramp intersects threshold level E_T marks the end of T_f and the beginning of T_n for the next operating cycle.

With the essential SCM ingredients identified, a control-loop block diagram is established next to guide the detailed analysis, from which the design for autocompensation of the LC parameters is made apparent.

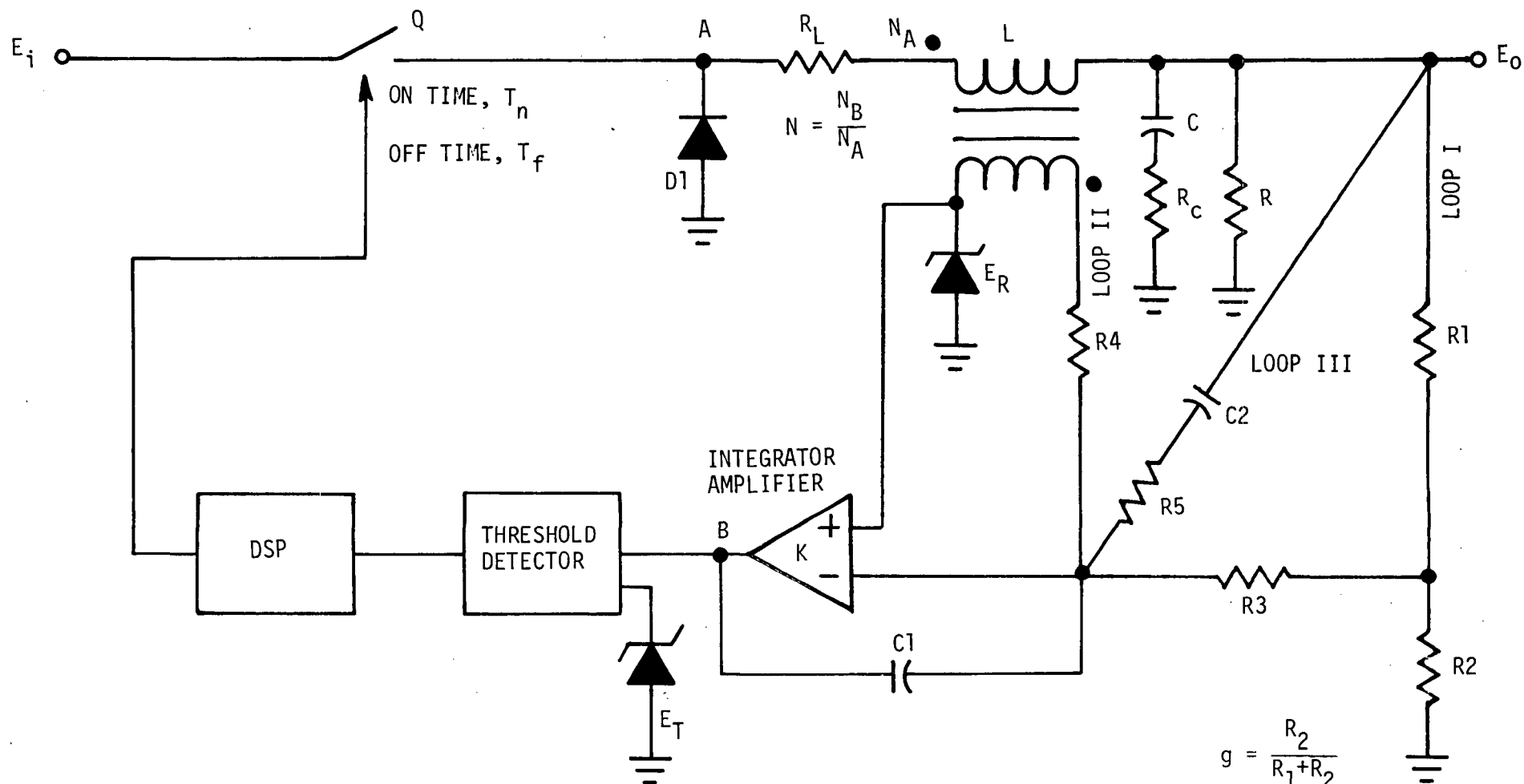


FIGURE 27. A SCM-CONTROLLED BUCK REGULATOR

7.1.2 A SCM-Controlled Power Processor Block Diagram

From the small-signal viewpoint, the power processor shown in Figure 27 can be separated into three parts shown in Figure 28A, B, and C. Starting at point A of Figure 27 and tracing clockwise, the output filter and load is illustrated in Figure 28A. Voltages e_1 and e_2 represent the filter output voltage and the inductor voltage respectively, which are source signals for loop I and II. These two voltages are applied to the integrator amplifier as depicted in Figure 28B, resulting in an integrator-amplifier output voltage e_B . A sinusoidal voltage perturbation of unity peak amplitude at point B will cause a corresponding pulse train at point A, with identical pulse amplitude E_i and on-time T_n , but with varying intervals for off-time T_f . The pulse train contains a fundamental component with peak amplitude K_p and with a frequency identical to that of the sinusoidal perturbation. The factor K_p is defined as the gain from B to A clockwise. The graphical representation of the aforescribed mechanism is shown in Figure 28C.

In Figure 28A, it can be shown that,

$$F_1(s) = \frac{e_1}{e_A} = \frac{\left(\frac{R}{R+R_L}\right)(1+SR_C C)}{1+S\left(\frac{R}{R+R_L}\right) \left[(R_L+R_C + \frac{R_L R_C}{R}) C + \frac{L}{R}\right] + S^2 LC \left(\frac{R+R_C}{R+R_L}\right)} \quad (16)$$

$$F_2(s) = \frac{e_2}{e_A} = \frac{SNL [1+SC (R+R_C)]}{(R_L+R) \left\{ 1 + \frac{SR}{R+R_L} \left[(R_L+R_C + \frac{R_L R_C}{R}) C + \frac{L}{R}\right] + S^2 LC \left(\frac{R+R_C}{R+R_L}\right) \right\}} \quad (17)$$

In Figure 28B, output e_B of the integrator is related to e_1 and e_2 by:

$$\frac{ge_1 - e_g - e_r}{R_3} + SC_1 (e_B - e_g - e_r) + \frac{e_1 - e_g - e_r}{R_5 + \frac{1}{SC_2}} + \frac{e_2 - e_g - e_r}{R_4} = 0 \quad (18)$$

Also, e_B is related to e_g by amplifier gain K ,

$$-Ke_g = e_B \quad (19)$$

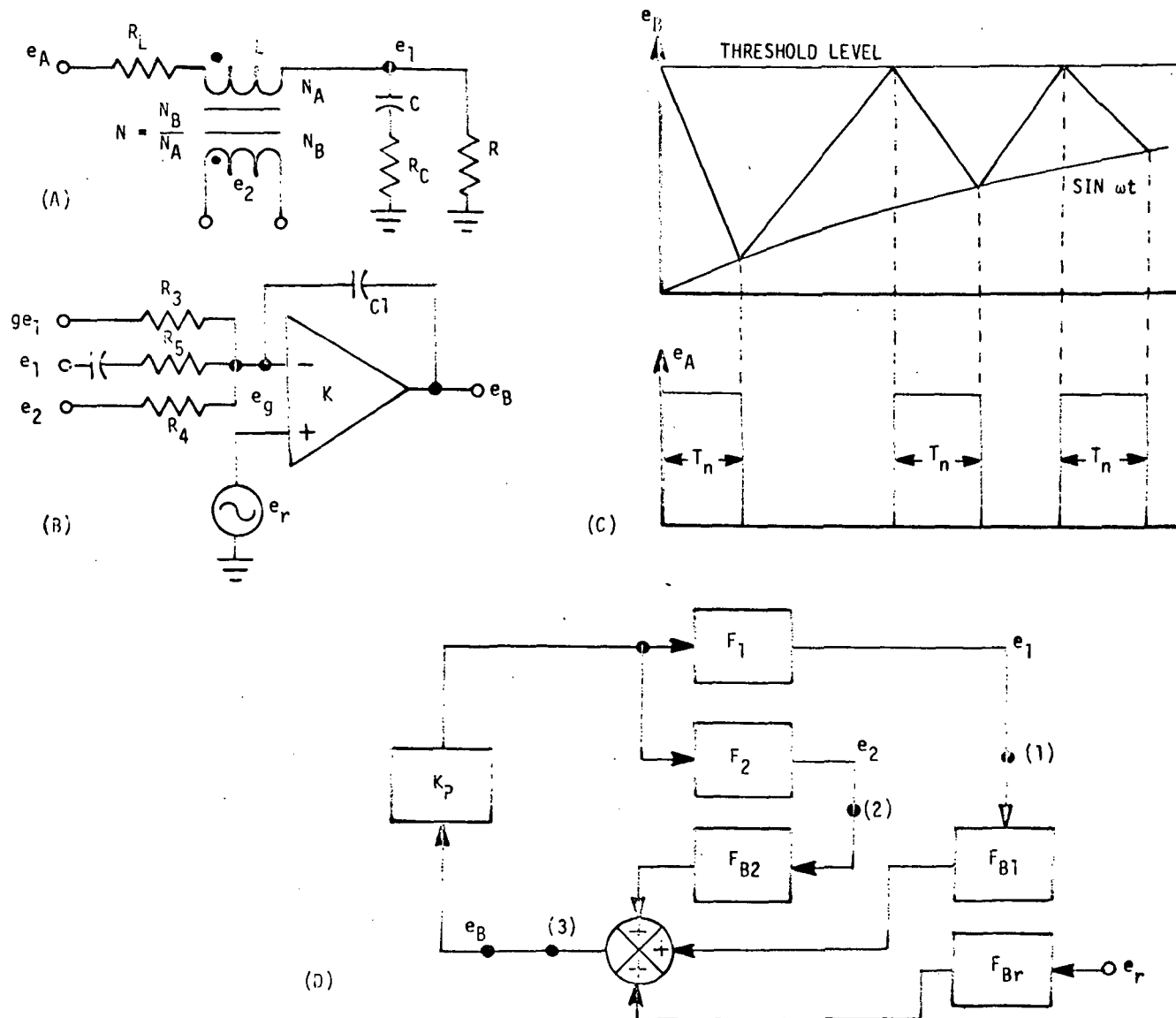


FIGURE 28. SMALL SIGNAL EQUIVALENT CIRCUIT OF A SCM-CONTROLLED BUCK REGULATOR

Combining (18) and (19) to eliminate e_g , one has

$$\begin{aligned}
 e_1 \left(\frac{SC_2}{1+SC_2R_5} + \frac{g}{R_3} \right) + \frac{e_2}{R_4} - e_R \left(\frac{1}{R_3} + SC_1 + \frac{SC_2}{1+SC_2R_5} + \frac{1}{R_4} \right) \\
 = - e_B \left[\frac{1}{KR_3} + SC_1 + \frac{SC_1}{K} + \frac{SC_2}{K(1+SC_2R_5)} + \frac{1}{KR_4} \right]
 \end{aligned} \tag{20}$$

Let F_{Br} , F_{B1} , and F_{B2} to represent $\partial e_B / \partial e_r$, $\partial e_B / \partial e_1$, and $\partial e_B / \partial e_2$, respectively,

$$F_{Br} = \frac{\frac{1}{R_3} + SC_1 + \frac{SC_2}{1+SC_2R_5} + \frac{1}{R_4}}{\frac{1}{K} \left(\frac{SC_2}{1+SC_2R_5} + \frac{1}{R_3} + \frac{1}{R_4} + SC_1 \right) + SC_1} \tag{21}$$

$$F_{B1} = - \frac{\frac{SC_2}{1+SC_2R_5} + \frac{g}{R_3}}{\frac{1}{K} \left(\frac{SC_2}{1+SC_2R_5} + \frac{1}{R_3} + \frac{1}{R_4} + SC_1 \right) + SC_1} \tag{22}$$

$$F_{B2} = - \frac{\frac{1}{R_4}}{\frac{1}{K} \left(\frac{SC_2}{1+SC_2R_5} + \frac{1}{R_3} + \frac{1}{R_4} + SC_1 \right) + SC_1} \tag{23}$$

Having identified the contribution of e_1 , e_2 , and e_r to e_B , the power processor control can be represented by the block diagram shown in Figure 28D. The five frequency-dependent blocks F_1 , F_2 , F_{B1} , F_{B2} , and F_{Br} , are expressed in eqs. (16), (17), (21), (22), and (23). The block K_p relates the integrator output to the voltage pulse train at the input of output filter, i.e., the pulses across free-wheeling diode D in Figure 27. The content of K_p will be analyzed later.

7.1.3 Open Loop Transfer Functions

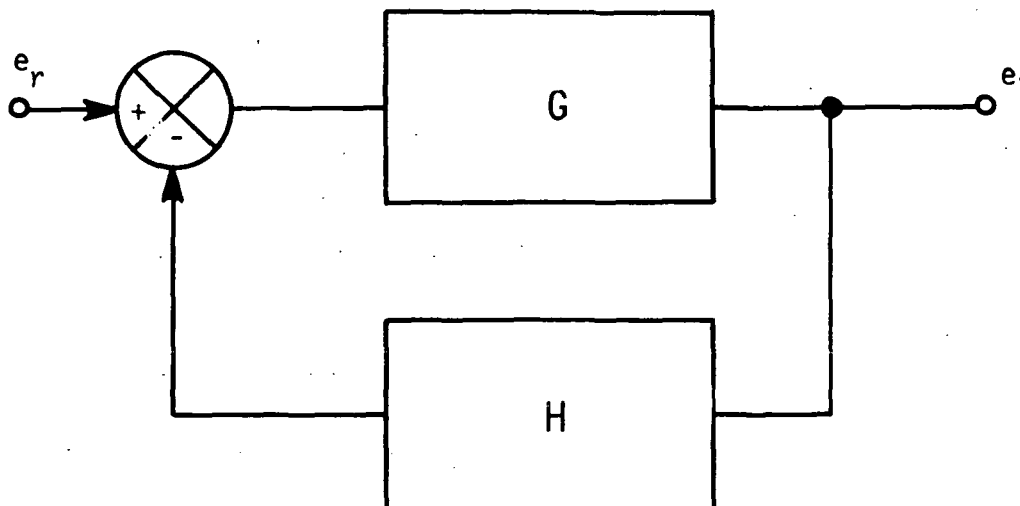
In Figure 28D, three locations are possible candidates as the breaking point to obtain the regulator system open-loop transfer function. They are marked numerically as points (1), (2), and (3), breaking the dc loop, the ac loop, and the composite dc- and ac-loop, respectively. The corresponding open-loop transfer functions can be obtained as:

$$(GH)_1 = - \frac{K_p F_1 F_{B1}}{1 + K_p F_2 F_{B2}} \quad (24A)$$

$$(GH)_2 = - \frac{F_1 F_{B1} + F_2 F_{B2}}{K_p} \quad (24B)$$

$$(GH)_3 = - K_p (F_1 F_{B1} + F_2 F_{B2}) \quad (24C)$$

To determine which of these three is meaningful in terms of SCM system stability, one starts by considering the block diagram of Figure 28D in relation to the generalized block diagram sketched below.



For a dc to dc switching regulator, the controlled variable is e_1 (the output voltage), and the reference input is e_r (the amplifier reference). By expressing e_1/e_r for Figure 28D, the logical choice for the breaking point can be identified from the equation $e_1/e_r = G/(1+GH)$.

With $e_2 = e_1(F_2/F_1)$, one has:

$$K_p F_1 [e_r F_{Br} + e_1 F_{B1} + (e_1 F_2/F_1) F_{B2}] = e_1 \quad (25)$$

from which one has:

$$\frac{e_1}{e_r} = \frac{K_p F_1 F_{Br}}{1 - K_p [F_1 F_{B1} + F_2 F_{B2}]} = \frac{G}{1 + GH} \quad (26)$$

The stability of the closed-loop system depends on the characteristic equation shown in the denominator of equation (26). Comparing (26) to (24) shows GH of (26) is identical to $(GH)_3$ in (24C), which leads to the conclusion that the system stability can only be studied by the open-loop transfer function when point (3) of Figure 28D is utilized as the loop breaking point.

Having identified point (3) of Figure 28D as the proper breaking point for stability study, then, upon making the following reasonable assumptions

$$K \gg 1$$

$$(1 + K) C_1 \gg C_2$$

$$R \gg R_L$$

$$R \gg R_C$$

and substituting equations (16), (17), (22), and (23) into (21), one obtains:

$$\frac{de_B}{de_A} = \frac{\left(\frac{-KgR_4}{R_3+R_4} \right) \left\{ (1+SR_C C) [1+SC_2(R_5+\frac{R_3}{g})] + S(1+SCR)(1+SC_2R_5) \frac{NR_3L}{gR_4R} \right\}}{\left\{ 1+S[(R_L+R_C)C + \frac{L}{R}] + S^2LC \right\} (1+SC_2R_5)(1+S \frac{KC_1R_3R_4}{R_3+R_4})} \quad (27)$$

Equation (27) can reveal the autocompensation of the LC parameters if for the time being one regards C_2 as negligibly small. Then, equation (27) is reduced to:

$$\frac{de_B}{de_A} = \frac{-\frac{KgR_4}{R_3+R_4} \left\{ 1 + S(R_C C + \frac{NR_3L}{gR_4R}) + S^2 \frac{NR_3LC}{gR_4} \right\}}{\left\{ 1 + S[(R_C+R_L) C + \frac{L}{R}] + S^2LC \right\} (1 + S \frac{KC_1R_3R_4}{R_3+R_4})} \quad (28)$$

One can note from equation (28) that if the factor (NR_3/gR_4) is designed so that

$$\frac{NR_3}{gR_4} = 1, \quad (29)$$

then, equation (28) is further simplified to

$$\frac{de_B}{de_A} = \frac{-\frac{KgR_4}{R_3+R_4} [1 + S(R_C C + \frac{L}{R}) + S^2LC]}{(1+S \frac{KC_1R_3R_4}{R_3+R_4}) \left\{ 1 + S[(R_C+R_L) C + \frac{L}{R}] + S^2LC \right\}} \quad (30)$$

From equation (30), the autocompensation of LC becomes clear, as both the numerator and denominator contain the S^2LC term. Both L and C can therefore vary extensively without effecting materially the open-loop transfer function. Even the first-order damping terms in the numerator and the denominator are fairly well matched, as they both contain L and C. Consequently, in most designs where unit (NR_3/gR_4) is observed, the (de_B/de_A) from A to B clockwise consists ideally a gain of $[KgR_4/(R_3+R_4)]$ and a first-order corner frequency $(R_3+R_4)/2\pi KC_1R_3R_4$.

It is noted that (de_B/de_A) of equation (27) only represents the transfer function from point A clockwise to point B of Figure 27. To complete the loop, the characteristic K_p from B clockwise to A must be derived. This is carried out in Appendix C. The open-loop transfer function of the SCM-controlled power processor is therefore,

$$G(s) = K_p \left(\frac{de_B}{de_A} \right) \quad (31)$$

where, K_p and (de_B/de_A) are expressed respectively in Appendix C and eq. (27).

It is also noted that equation (30) revealing autocompensation is based on a negligibly small C_2 in equation (27). In practical applications C_2 is not negligibly small, and it tends to detract the SCM control from achieving the intended autocompensation. The need for C_2 has been discussed in Section 4.4, and the impact of C_2 on stability are presented in Appendix D, which includes the complete open-loop transfer function and the supporting computer analysis.

The discussion thus completes the stability aspect of the SCM, with emphasis on autocompensation of the output-filter parameters. The contribution of the AC loop to the autocompensation is apparent from equation (28) if one diminishes the AC-loop effect by letting N approach zero.

Another characteristic provided by the AC loop is the instantaneous duty-cycle formation in responding to a step input-voltage change. This aspect has been discussed in Section 4.4.

7.2 SCM-CONTROLLED REGULATOR TIME-DOMAIN MODELING

The objective of time-domain modeling and analysis is to match the universal capability of SCM hardware by developing a unified, generalized method of control-loop analysis. The analysis, therefore, should be distinguished by the following characteristics:

- Applicable to all types of switching regulators
- Preserve the effect of different duty-cycle control on regulator performances
- Applicable to continuous- and discontinuous-current in the output filter inductor
- Exact description of regulator state variables at any given instant to maintain analytical accuracy.

Needless to say, such an analysis would provide a ready foundation for establishing a cost-effective computer simulation program that actually portrays the regulator switching under steady-state and dynamic operations.

The generalized time-domain approach, based on state space techniques, is described next.

7.2.1 Generalization of the Discrete Time, Time Domain Approach to Regulator Modeling and Analysis

Most switching regulators operate on the principle of controlling the duty cycle with which a primary source is switched to a load, or to an energy-storage element interfacing between the source and the load, in a manner so that a constant load voltage or current is maintained. Thus for some period of time the power switch is on, and for some period it is off, repeating this duty cycle over and over. However, unless the regulator is in its steady-state and in a disturbance-free environment, the on and off times and the duty cycle are not constant and the models presented here do not make this assumption. In fact, it is of paramount importance for successful simulation and analysis to properly model the mechanisms producing these changes in the on- and/or off-time intervals.

This modeling is done by describing the regulator with two or more linear time-invariant systems, each valid over a certain, well defined period within a cycle. A state vector $\bar{x}$ is defined, which typically is comprised of the voltages or currents describing the state of energy-storage devices in the regulator. Figure 29 shows the inductor current i_L of a hypothetical regulator (say, a series buck regulator), and serves here merely the purpose of establishing notation regarding time instances. Each cycle is divided into three different operational conditions:

$t_k \leq t < t_1^k$, transistor off, diode on, nonzero inductor current

$t_1^k \leq t < t_2^k$, transistor off, diode off, zero inductor current

$t_2^k \leq t < t_{k+1}$, transistor on, diode on, nonzero inductor current

Note that the second time interval vanishes when the filter inductor current is continuous. Note also that all time periods T_i in Figure 29 are also indexed by k in the form of a superscript; they may vary from cycle to cycle, as during a transient condition, for instance. The regulator containing three states would then be described by three linear differential equations given in state vector notation as

$$\dot{\bar{x}} = F_1 \bar{x} + G_1 \bar{U}_1, \quad t_k \leq t < t_1^k \quad (32)$$

$$\dot{\bar{x}} = F_2 \bar{x} + G_2 \bar{U}_2, \quad t_1^k \leq t < t_2^k \quad (33)$$

$$\dot{\bar{x}} = F_3 \bar{x} + G_3 \bar{U}_3, \quad t_2^k \leq t < t_{k+1} \quad (34)$$

In these equations, F_i and G_i , with $i = 1, 2, 3$, are constant matrices of appropriate dimensions, and $\bar{U}_i$, with $i = 1, 2, 3$, denotes a vector comprised of piecewise constant voltages, typically the supply voltage E_i and the regulator reference voltage E_R . Note that the three systems need not be identical, since the matrices are free to differ from each other. This is particularly important for discontinuous current operation and buck-boost and boost regulators. In addition, threshold conditions must be specified

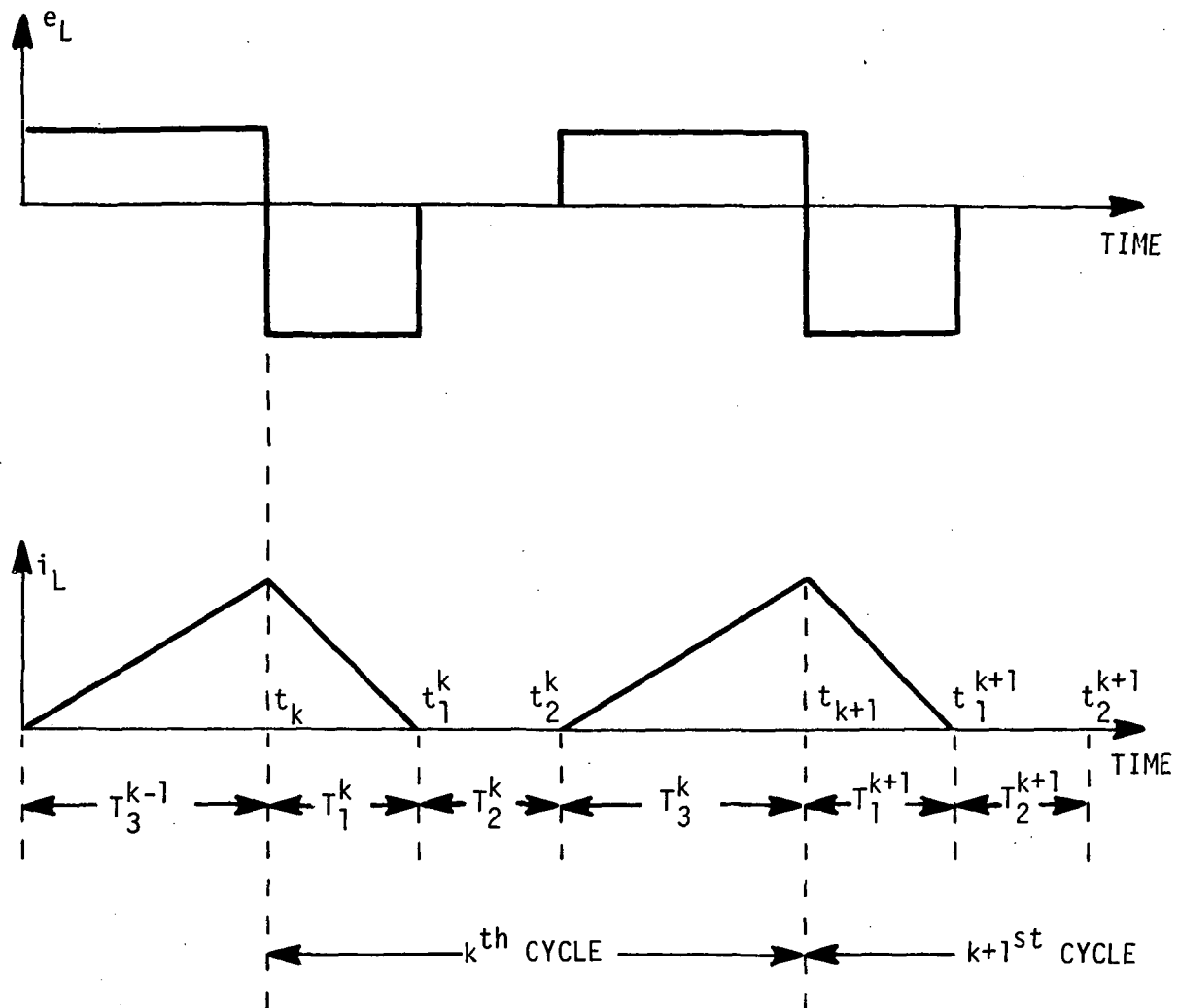


FIGURE 29 THE THREE STATES OF DISCONTINUOUS-INDUCTOR-CURRENT OPERATION

which define when the time instances t_1^k and t_2^k occur. For instance, suppose the state x_2 represents the power stage inductor current. The threshold condition for t_1^k may then be described by

$$x_2(t_1^k) = 0, \quad (35)$$

since no negative current flow is allowed. Similarly, the threshold condition on t_2^k may be described by

$$x_3(t_2^k) = E_T = \text{threshold voltage}, \quad (36)$$

and on t_{k+1} possibly as

$$T_3^k = T_n = \text{constant} \quad (37)$$

The main user interface with such a analysis program is to supply the number of different circuit conditions, say m per cycle, the dimensions and entries of the matrices F_i , G_i , $i = 1, 2, \dots, m$, the dimension and entries for the input vectors $\bar{u}_i$, $i = 1, 2, \dots, m$, and the threshold conditions equivalent to equations (35) to (37), which could be expressed in standard form as

$$h_i(\bar{x}(t_i^k), T_i^k, \bar{u}_i, \bar{p}) = 0, \quad i = 1, 2, \dots, m \quad (38)$$

where $\bar{p}$ is a vector of other converter parameters such as threshold voltages and constant time periods.

Each of the linear systems of equations (32) to (34) admits a closed form solution of the form

$$\bar{x}(t_1^k) = \bar{x}(t_k + T_1^k) = \Phi_1(T_1^k) \bar{x}(t_k) + D_1(T_1^k) \bar{u}_1 \quad (39)$$

$$\bar{x}(t_2^k) = \bar{x}(t_1^k + T_2^k) = \Phi_2(T_2^k) \bar{x}(t_1^k) + D_2(T_2^k) \bar{u}_2 \quad (40)$$

$$\bar{x}(t_{k+1}) = \bar{x}(t_2^k + T_3^k) = \Phi_3(T_3^k) \bar{x}(t_2^k) + D_3(T_3^k) \bar{u}_3 \quad (41)$$

where the state transition matrices ϕ_i are given by

$$\phi_i(T) = e^{F_i T}, \quad i = 1, 2, 3 \quad (42)$$

and the input matrices D_i by

$$D_i(T) = e^{F_i T} \left[\int_0^T e^{-F_i s} ds \right] G_i, \quad i = 1, 2, 3 \quad (43)$$

For simple, low order systems the matrices $\phi_i(T)$ and $D_i(T)$ can often be analytically evaluated as algebraic functions of T , as was the case in the work reported in Reference [22]. But for a general analysis program applicable to a variety of converter configurations (some of possibly high order), the matrices $\phi_i(T)$ and $D_i(T)$ will be evaluated numerically by the computer. The matrix exponential of equation (42) is evaluated from its series representation, i.e.,

$$e^{FT} = I + FT + \frac{F^2 T^2}{2!} + \frac{F^3 T^3}{3!} + \dots \quad (44)$$

with the number of terms to be added up being determined by an error criterion. Computation of $D_i(T)$ is then straightforward using trapezoidal or Runge-Kutta integration over the interval $[0, T]$. The computation of $\phi_i(T)$ and $D_i(T)$ would be programmed as a FUNCTION SUBPROGRAM with T as a formal parameter so that $\phi_i(T)$ and $D_i(T)$ could be evaluated for any specified T .

The threshold conditions are used to define the time periods T_i^k , $i = 1, 2, \dots, m$. For instance, the threshold condition of equation (35), $x_2(t_1^k) = 0$, becomes by equation (39)

$$\begin{aligned} & \phi_{21}^1(T_1^k) x_1(t_k) + \phi_{22}^1(T_1^k) x_2(t_k) + \dots + \phi_{2n}^1(T_1^k) x_n(t_k) \\ & + d_{21}^1(T_1^k) u_1^1 + d_{22}^1(T_1^k) u_2^1 = 0 \end{aligned} \quad (45)$$

In effect then, all T_i^k , $i = 1, 2, \dots, m$ can be represented as functions of the system state at t_k and other known converter parameters and inputs, i.e., as algebraic functions of the form

$$z_i(\bar{x}(t_k), T_i^k, \bar{u}_i, \bar{p}) = 0 \quad i = 1, 2, \dots, m \quad (46)$$

The nonlinear discrete-time system that describes the converter behavior exactly, can now be obtained by combining the closed form solutions. For equations (39) - (41), which represent an example where $m = 3$, the result is the following vector difference equation

$$\begin{aligned} \bar{x}(t_{k+1}) = & \phi_3(T_3^k) \left\{ \phi_2(T_2^k) \left[\phi_1(T_1^k) \bar{x}(t_k) + D_1(T_1^k) \bar{u}_1 \right] + D_2(T_2^k) \bar{u}_2 \right\} \\ & + D_3(T_3^k) \bar{u}_3 \end{aligned} \quad (47)$$

which can be written in short form as

$$\bar{x}(t_{k+1}) = \bar{f}(\bar{x}(t_k), T_1^k, T_2^k, T_3^k, \bar{u}_1, \bar{u}_2, \bar{u}_3) \quad (48)$$

The time periods T_i^k are all functions of the current system state $\bar{x}(t_k)$ by virtue of the threshold conditions (46), and thus (46) and (48) together are a nonlinear discrete-time system with the state vector $\bar{x}$ describing the behavior of the power converter at one instant of time for each cycle. Typically this instant represents either the limit cycle peak value or the minimum value of the output voltage. The nonlinear discrete time system (46) - (48) is of key importance for stability and transient analysis.

The steady state equilibrium solution $\bar{x}^*$ of the nonlinear discrete-time system (48) is defined by the condition

$$\bar{x}(t_{k+1}) = \bar{x}(t_k) = \bar{x}^* = \text{constant} \quad \text{for all } k = 0, 1, 2, \dots \quad (49)$$

and it must be determined first. It represents the numerical value at the time instances t_k of the steady state limit cycle of the regulator, usually the limit cycle peak value. Amplitude and frequency of the limit cycle can be determined from it. The nonlinear system (48) is then linearized about its equilibrium $\bar{x}^*$ and a linear, time-invariant, discrete-time system is obtained which is characterized by the vector difference equation

$$\delta \bar{x}(t_{k+1}) = \Psi \delta \bar{x}(t_k) \quad (50)$$

where $\delta\bar{x} = \bar{x} - \bar{x}^*$. This system describes the regulator behavior about its steady state solution and it is stable, if and only if, all the eigenvalues of the constant $n \times n$ matrix Ψ are absolutely less than unity, i.e.,

$$|\lambda_i(\Psi)| < 1, \quad i = 1, 2, \dots, n \quad (51)$$

Changes in the eigenvalues (which are the roots of the system) due to system parameter changes can be plotted in the complex plane yielding an excellent design tool, very similar to conventional root locus plots widely used in control system design. The location of the roots does not only indicate stability or instability of the system, but also characterizes its transient behavior, i.e., damping, overshoot and rapidity of response. For stability, all the roots must be inside the unit circle in the complex plane.

The matrix Ψ is the Jacobian of (48) evaluated at $\bar{x}^*$, i.e.,

$$\Psi = \left. \frac{\partial \bar{f}}{\partial \bar{x}} \right|_{\bar{x}^*} \quad (52)$$

where it must be kept in mind that T_i^k , $i = 1, 2, \dots, m$, are functions of $\bar{x}(t_k)$ via the threshold conditions of equation (46). In order for the analysis program to be general and require no complicated user interactions, the partials in (52) are evaluated numerically by approximating them by difference quotients. This technique has been described in Reference [22].

The linearized system (50) can also be used to assess the regulator's audiosusceptibility and to investigate the transient behavior caused by line or load step changes. It can be seen then that the discrete-time, time domain approach is a very useful tool for power regulator modeling and analysis.

7.2.2 Application of the Generalized Approach to A Continuous-Current Buck Regulator with Constant - T_n SCM Control

Based on the generalized analytical approach outlined in the previous section, a buck regulator controlled by a constant- T_n SCM and operated under a continuous filter inductor current is analyzed for stability and audio-susceptibility. Key analytical efforts include the following:

- Formulation of state equations
- Derivation of equivalent nonlinear discrete time system
- Numerical iteration to determine exact steady-state equilibrium solution
- Linearization of the nonlinear, discrete time system
- Stability analysis of the linearized system
- Study of audio-susceptibility performance
- Study of output transient caused by a step change in supply voltage
- Experimental verification of analytical results.

Details of this work was presented in the 1975 IEEE Power Electronics Specialists Conference, Los Angeles, California. The paper is included herein as Appendix E.

7.2.3 Application of the Generalized Approach to a Continuous-Current Buck Regulator with Constant-Frequency SCM Control

Essentially following the same procedures described in Appendix E for the constant- T_n SCM, the buck regulator operating in the constant-frequency mode is analyzed. The system investigated here uses the constant-frequency clock pulses to initiate the on-time interval; the on time is terminated by the ramp-threshold intersection. The main result of the analysis is that no circuit parameter change was able to stabilize the regulator for duty cycles higher than 50%, which confirms the previous experimental observation and the graphical interpretation advanced in Section 4.6.

The analysis shows the regulator to be unstable with a supply voltage of 30V and a reference voltage of 20V (i.e., for an approximate duty cycle of 0.67). While changes in such critical parameters as dc feedback and ac feedback affected the system roots in one way or another, the only really effective parameter change for stabilizing the system was to decrease the duty cycle, i.e., to either increase supply voltage E_i or to decrease the desired output voltage E_R .

Figure 30 shows a root locus plot as a function of supply voltage E_i , with E_R remaining constant at 20V. As can be seen, increases in E_i primarily move the negative real root toward the unit circle, and at a value of $E_i = 46V$, i.e., a duty cycle of 0.435, the system is just barely stable. Its difference from the 0.5 theoretical limit predicted in Section 4.6 is likely due to the effect of C2 used for transient-response improvement. This capacitance couples the switching-frequency voltage ripple at the converter output to the integrator, causing the integrator output ramp to deviate from the ideal triangular waveform. Since the 0.5 stable duty-cycle limit is based on an ideal integrator output ramp, it is not surprising that the modified integrator ramp including the effect of output ripple should result in a duty-cycle limit that is slightly different. To prove this assertion, the duty cycle was kept at 50% by choosing $E_i = 40V$. The filter inductance L_o was increased, and capacitance C2 was decreased, both having the same effect of reducing the effect of output ripple on the integrator ramp. When that happened, the root approached the -1 point asymptotically as L_o becomes larger and larger. The 50% duty cycle as a critical stability limit is thus confirmed.

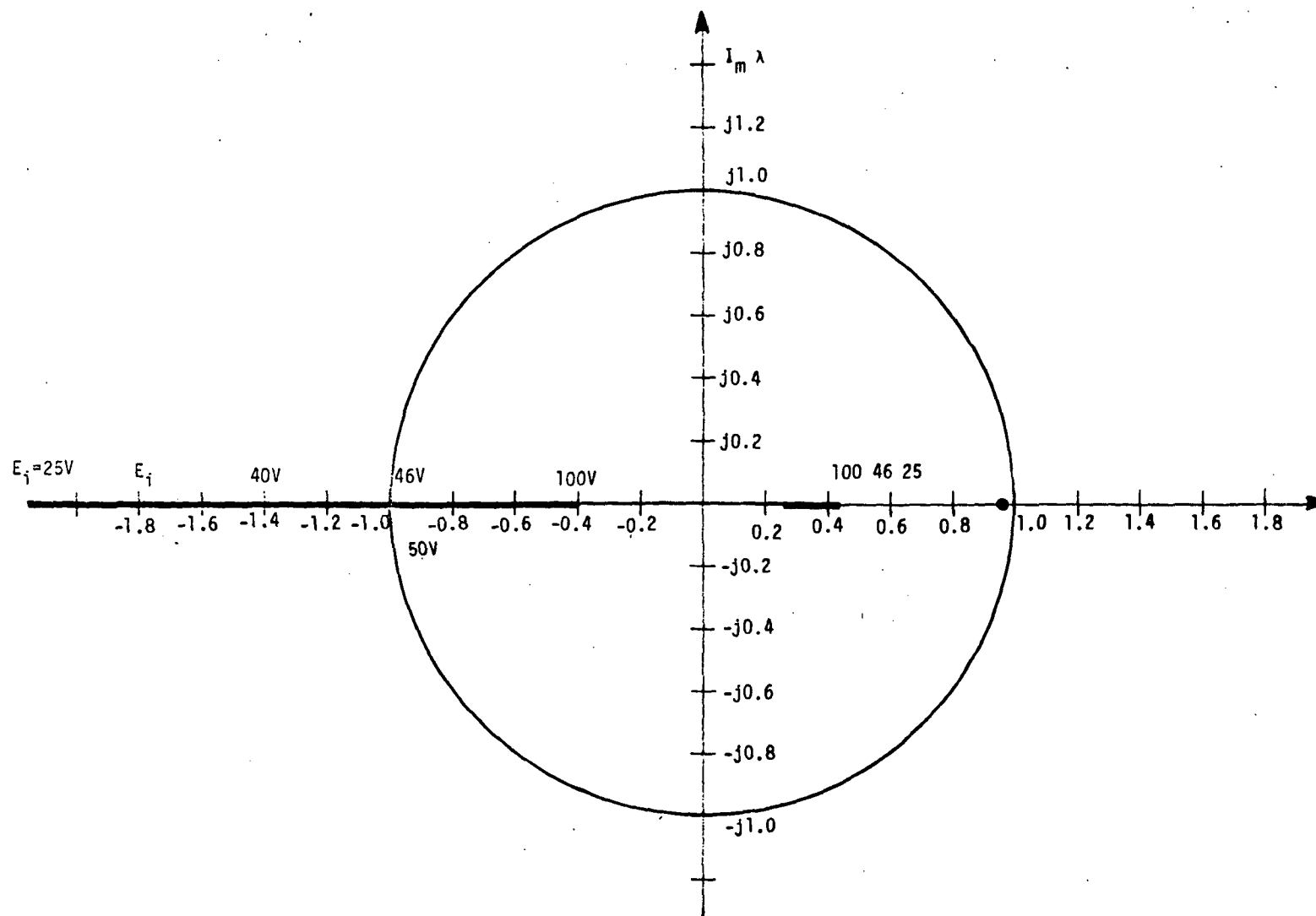


FIGURE 30. ROOT LOCUS PLOT AS A FUNCTION OF SUPPLY VOLTAGE

7.3 COST-EFFECTIVE DIGITAL SIMULATION

The above described time domain approach to system modeling and analysis is particularly well suited for digital simulation of a regulator. The simulation is based on the closed form solutions (39) - (41). The time step T can be specified as a fraction (including unity) of the steady state values of the time periods T_i , $i = 1, 2, 3$. Thus, using the closed form solutions, the system state can be propagated by constant state transition matrices until either a threshold condition has been transgressed or a fixed, known time period has elapsed. In the former case, after exceeding the threshold, iterative linearization (Newton's method) of the threshold is used to determine the exact time instant when the threshold has been reached and a new circuit condition exists, i.e., when one has to switch to a different state transition matrix, a different input matrix, or a new input vector.

The use of the closed form solutions is very important for speeding up the simulation run-time, since otherwise, because of the low system damping and the switching discontinuities, very small integration steps would have to be used. This technique of digital simulation of a switching regulator has been applied to the SCM with very good results, demonstrating that digital computers are well suited for simulating regulator systems. The cost of machine plotting the simulation results will usually exceed the central processor cost of running the simulation. A good rule of thumb is that most runs, inclusive plotting and time-share terminal time, will cost about \$2.00 per run.

Another advantage of simulation based on closed-form solutions is settling time required for steady-state waveform. In programs such as ECAP and SCEPTRE, the difficulty in assuming matched initial conditions for all state variables often cause the system to engage in prolonged oscillation before the equilibrium steady-state is reached. This drawback is not shared by simulation based on closed-form solutions.

A sample simulation program is given in Appendix F, in which the steady-state and transient performances of a buck regulator operating with constant- T_n are simulated. The cost-effectiveness of the simulation is dramatically reflected in run No. 2 of Appendix F. A 3.5-second Central Processor Time is all it takes to simulate the required steady-state waveform. Similar systems simulated previously in another project by using SCEPTRE took six minutes. A time saving of two order of magnitudes is thus achieved.

7.4 RECOMMENDED FUTURE SCM MODELING AND ANALYSIS OBJECTIVE

Future activities in SCM modeling and analysis must be aimed to promote SCM utilization among regulator engineers who are actively involved in the various aspects of design application and project management. The most effective promotion is to enable a power-processor engineer to design readily the needed SCM control-circuit parameters, and to confidently predict that the regulator performances based on such a design would satisfy the specified requirements.

It is immediately apparent such an endeavor transcends the effort normally involved in a task whose singular objective is to provide only the control-loop analysis. Rather, the ultimate goal here is to provide the control design as a function of control requirements - a design so intrinsically based on comprehensive analytical results that the confidence on such a SCM design to meet all requirements indeed can be upheld without further analysis by the prospective SCM user.

To achieve this goal, extensive analysis must be a prerequisite. Based on the analytical results, useful design information can then be formulated for the user. Such an effort must comprise the following activities:

- Fully define the necessary contents of design information from the User's viewpoint.
- Analytically characterize the regulator functional blocks that include all basic power configurations, all duty cycle control modes, and the SCM error processor.
- Analyze the regulator performances based on linear/nonlinear models thus obtained.
- Extract qualitative relationships between design parameters and corresponding performances, and formulate design guidelines to meet a given set of performance requirements that includes stability, audiosusceptibility, output impedance, and step transient responses.

Successful conclusion of these efforts will result in a "SCM design handbook," thus reducing the design of SCM-controlled switching regulators to a routine task. Such a contracted effort (NAS3-20102), "Application Handbook for a Standardized Control Module for DC-to-DC Converters," has been funded. Work towards obtaining and publishing such a handbook is now underway.

8. CONCLUSION

The standardized Control Module (SCM) was utilized successfully as the controlling element for three most commonly used switching regulators: the buck boost, the series buck, and the parallel-inverter converter. Major merits of the SCM can be summarized in terms of the standardization aspect and the performance aspect:

Standardization

- Capable of performing various duty cycle control means using a standardized control circuit.
- Applicable to all switching regulators regardless whether the output-filter inductor current is continuous or discontinuous.
- Built-in features providing all conceivable control, command, protection, and isolation functions.
- Basic Control Module incorporating the standardized analog signal processor and digital signal processor is interchangeable among different switching regulators.

Performance

- Regulator stability between 0 to 100% duty cycle is accomplishable, which can be made relatively immune to output-filter parameter changes when compared to conventional single-loop control.
- Peak-stress limiting for all power components during all conceivable line/load transients including regulator starting and output fault.
- High dc gain and within 0.1% dc output regulation under wide line, load, and temperature variations (2-to-1 input voltage change, open load to full load, and -25° to $+85^{\circ}\text{C}$).
- Dynamic output regulation under wide line and load step or sinusoidal disturbances to be within the 1% ripple specification.

These merits are further complemented by the SCM modeling and analysis accomplished to date, which has encompassed both the classical frequency-domain transfer function and the modern time-domain state-space techniques. In fact, the universal capability of the SCM hardware is matched in software by the development of a generalized nonlinear discrete-time system modeling and analysis, which has proved to be cost-effective and accurate in performance analysis and simulation.

In summary, these accomplishments have greatly enhanced the utility of the control circuit as a Standardized Control Module for high-performance

power processors. Furthermore, effort is already underway to compile a SCM design handbook which, upon its completion, will enable a prospective SCM user to design readily the various SCM circuit parameters in order to meet a set of specified performance requirements. A regulator design will then become a routine task insofar as the control-dependent performances are concerned.

It is therefore our hope that this control module will soon find its way into various military and space applications. The standardized circuit configuration, in conjunction with established design guidelines, will certainly contribute to savings in power-processor design, development, analysis, and manufacturing cost.

9. APPENDICES

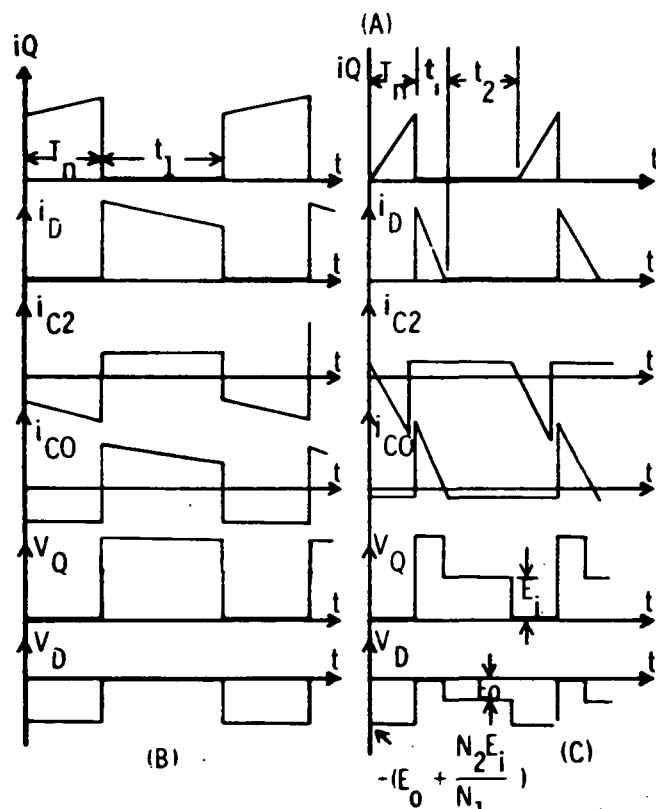
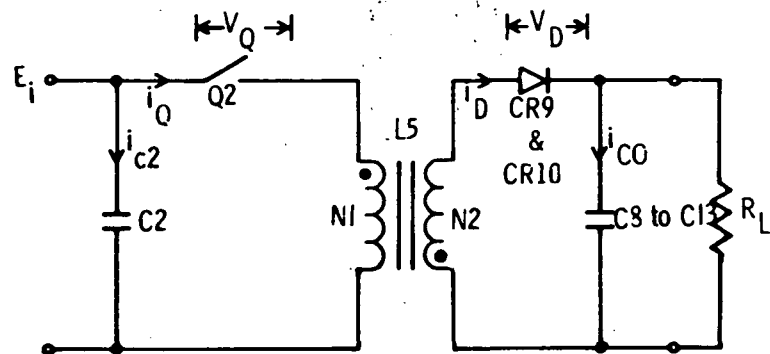
The following is a list of appendices, which are included herein to complement the technical discussion presented in the previous sections:

- Appendix A. Basic Power Circuit and Demonstration Breadboard Descriptions
- Appendix B. Summary of Dc-Dc Converter requirements.
- Appendix C. Gain of Pulse Modulation Stage
- Appendix D. The Effect of Transient-Response Improvement on SCM Stability
- Appendix E. Time Domain Modeling and Stability Analysis
- Appendix F. Cost-Effective Time Domain Simulation

APPENDIX A

BASIC POWER CIRCUIT AND DEMONSTRATION BREADBOARD DESCRIPTIONS

(1) CIRCUIT AND WAVEFORM (BUCK BOOST)



In Figure (A), the energy-storage inductor utilizes a core which has a fairly linear flux vs MMF characteristic. Energy is derived from the power source (in this case through the input filter), and stored inductively in the inductor during on-time interval T_n when power transistor Q2 is conducting. When it is turned off, a current flow through the inductor secondaries must occur, since the MMF of the core cannot change instantaneously. Thus the energy previously stored in the primary inductance during T_n is delivered from the secondary winding during the off half cycle, T_f , as output energy. Through fast recovery diodes CR9 and CR10, the energy is received by the load and filter capacitors C8 through C13. Notice that the energy is delivered to the output in the form of a series of unidirectional current pulses, allowing the output filter to be merely capacitors.

Depending on the line and load conditions, the operating waveforms for a given design can have either a non-zero MMF in the inductor at heavy load, or a zero MMF during a portion of the power switch off time in each cycle at light load.

These two conditions are shown in Figures (B) and (C).

(2) DESIGN CRITERIA (BUCK BOOST)

Based on relationships for volt-second balance on the inductor and energy balance for the converter, time intervals t_1 and t_2 are derived in terms of T_n , input E_i , output E_o , and load resistance R_L , where

$$t_1 = \frac{E_i T_n}{E_o} \frac{N_2}{N_1}$$

$$t_2 = \frac{e E_i^2 R_L T_n - 2 L_p E_o (E_o + \frac{N_2 E_i}{N_1})}{2 L_p E_o^2} T_n$$

Here, e is the efficiency, and L_p is the primary inductance of the converter. Notice that a critical $R = R_k$ exists, below which t_2 becomes negative, i.e., physically unrealizable. This resistance value can be predicted by letting t_2 be zero, and solving for R_L , where

$$R_L = R_k = \frac{2 L_p E_o (\frac{E_o}{E_i} + \frac{N_2}{N_1})}{e E_i T_n}$$

The period of T for each steady-state cycle is:

$$T = T_n + t_1 = T_n (1 + \frac{E_i N_2}{E_o N_1}), R_L \leq R_k$$

$$T = T_n + t_1 + t_2 = \frac{e R_L (E_i T_n)^2}{2 L_p E_o^2} = \frac{e (E_i T_n)^2}{2 L_p P_o} \quad R_k < R_L$$

where $P_o = E_o^2 / R_L$ is the converter output power.

In this design, $T \approx 40 \mu s$ for $R_L \leq R_k$.

Tradeoff studies were undertaken to identify the optimum power circuit design. The study results indicated that, with the specified line and load ranges, the design giving a zero t_2 at heavy load and a non-zero t_2 at light load, would provide the highest efficiency and minimum weight. To carry out this design philosophy, the threshold between zero and non-zero t_2 is set to occur at a converter input voltage of 20V and an output corresponding to one-third of the full load.

With an input voltage variation between 20V to 40V and a regulated output voltage at 28V, a unity turns ratio for N_1 and N_2 becomes attractive for two reasons: (1) Such a turns ratio will cause a duty cycle that does not approach zero or unity, thus relieving the switching characteristic requirements of semiconductors and leaving ample time to reset various magnetics; (2) Such a turns ratio facilitates the use of bifilar windings for N_1 and N_2 . With $N_2/N_1 = 1$, $E_o = 28V$, $e = 0.9$, $E_i = 20V$, $E_i T_n = 560 \times 10^{-6}$ vs, and $R_k = 60$ ohms (i.e., about one-third of full load), inductance L_p is calculated to be $220 \mu H$.

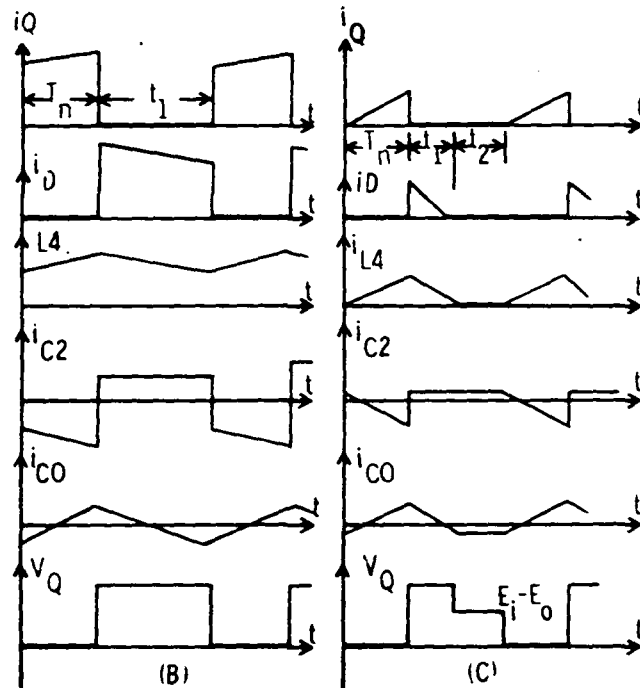
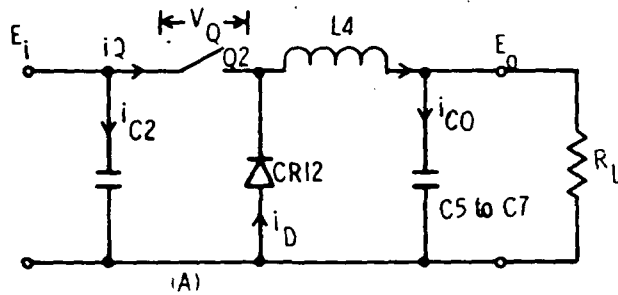
Using the same notation, the peak flux density in the core, B_p , is

$$B_p = \frac{P_o}{e E_i} \frac{L_p}{N_1 A} (1 + \frac{N_2 E_i}{N_1 E_o}) + \frac{E_i T_n}{2 N_1 A}, \quad A = \text{core area}$$

To reduce the core loss, a ferrite toroid with cut gaps along its diameter was selected to achieve the desired permeability. The converter efficiency improvement as a result of changing to the ferrite core was calculated to be about one percent.

For a given inductor and a specified $E_i T_n$, the steady-state power rating of the transistor and the diode are readily determined from the worst-case voltage and current over the range of line and load variations. Other selection criteria include the current gains, the conduction voltage drop, the switching characteristic and its effect on control circuit noise susceptibility, the storage time, and the secondary breakdown susceptibility.

From a weight viewpoint only, a C-L-C filter is more attractive than a capacitor filter. However, the capacitor filter is superior with respect to its power loss and its output impedance, and is selected for the design. AC capacitors with negligible ESR's, such as the polycarbonate type, were considered but not chosen, due to their excessive size and weight. Six tantalum-foil capacitors in parallel, with $100 \mu F$ each, are then chosen to meet the 1% peak-to-peak output ripple requirement at the cold environment ($-25^\circ C$) when the ESR of the capacitor is the highest.

(1) CIRCUIT AND WAVEFORMS (SERIES BUCK)

In Figure (A), transistor Q2 is controlled by the ASDTIC module to turn on and off cyclically for respective time intervals T_n and T_f . During T_n , CR12 is reverse biased, and E_i is applied to the output filter. During T_f , CR12 conducts to maintain the MMF continuity in $L4$, and an essentially zero voltage is applied to the filter. After averaging by the filter, a dc output voltage E_o is obtained.

(2) DESIGN CRITERIA (SERIES BUCK)

In the subject converter, the control circuit is implemented in such a way that time interval T_n is inversely proportional to input voltage E_i , or,

$$T_n = \frac{\text{Constant}}{E_i}$$

Based on relationships for volt-second balance on the inductor and energy balance for the converter, time intervals t_1 and t_2 are derived in terms of T_n , E_i , E_o , and R_L , where

$$t_1 = \frac{E_i - E_o}{E_o} T_n$$

$$t_2 = \frac{dR_L E_i^2 (E_i - E_o) T_n - 2L E_i E_o^2}{2L E_o^3} T_n$$

Here, e is the efficiency, and L is the filter inductance. Notice that a critical $R_L = R_k$ exists, below which t_2 becomes negative, i.e., physically unrealizable. This resistance value can be predicted by letting t_2 be zero, and solving for R_L , where

$$R_L = R_k = \frac{2LE_o^2}{eE_i T_n (E_i - E_o)}$$

From equations representing T_n , t_1 , and t_2 , the period T of a steady-state cycle is

$$T = T_n + t_1 = \frac{E_i T_n}{E_o}, \quad R_L \leq R_k$$

$$T = T_n + t_1 + t_2 = \frac{e \left(\frac{E_i}{E_o} - 1 \right) (E_i T_n)^2}{2LP_o}, \quad R_k < R$$

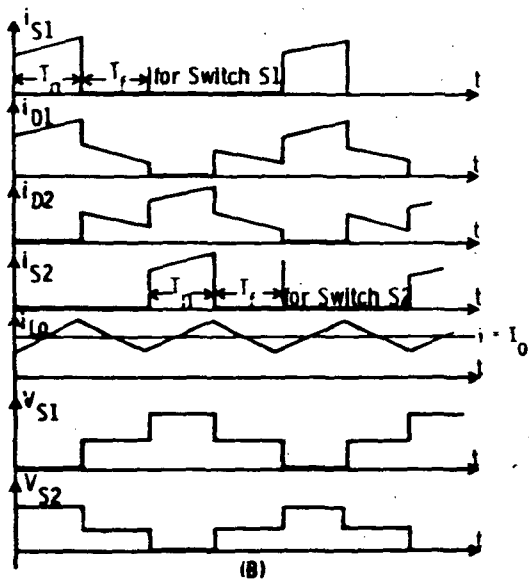
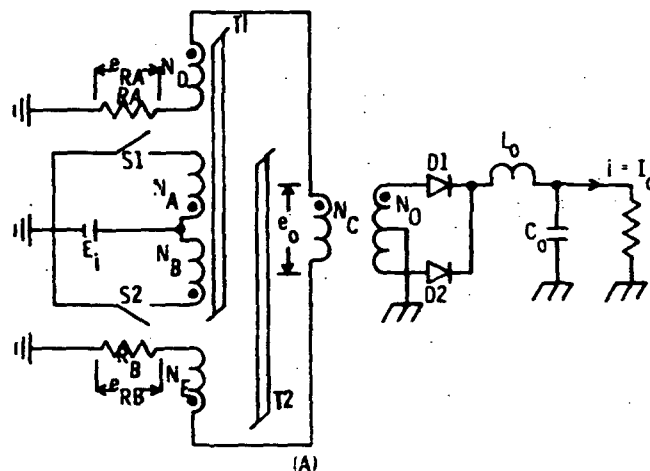
where $P_o = E_o^2 / R_L$ is the converter output power. In this design,

$$T \cong 30 \mu s \text{ for } R_L < R_k$$

Similar to the buck-boost converter, the approach for $t_2 = 0$ at heavy load and $t_2 > 0$ at light load yields optimum efficiency and weight. The threshold between zero and non-zero t_2 is designed to occur at an input of 32V and an output corresponding to one-third of the full load. With $E_o = 20V$, $e = 0.92$, $E = 32V$, $E_i T_n = 600 \times 10^{-6} \text{ VS}$, and $R_k = 30 \text{ ohms}$, inductance L is calculated to be approximately 250 μH .

The peak-flux density in the core is:

$$B_p = \frac{LP_o}{NAE_o} + \frac{(E_i - E_o) T_n}{2NA}$$

(1) CIRCUIT AND WAVEFORM (PARALLEL INVERTER)

In pulsewidth modulation (PWM) converter shown in Figure 13, each of the two switches, S1 or S2, is controlled to turn on and off cyclically; conduction of both S1 and S2 are mutually-exclusive events. The LC filter of each output receives an input voltage corresponding to $(N_A/N_B) V_o$ during T_{on} , and receives an essentially zero voltage during T_{off} . This voltage pulse train is averaged by the output filter to yield the required output voltage.

The utility of high-power parallel inverter has been hampered by high-stress conditions caused by the saturation of the power transformer. Saturation is either necessary to turn off the conducting switch, [29] or it is inevitable due to asymmetry between the two inverter halves. The asymmetry cyclically impresses a differential volt-second increment to the core, resulting in its ultimate saturation at one end of its BH loop. Even when a saturation sensor is used, the inability of the transistor switch to turn off immediately after detection of saturation by the sensor (due to signal delay and the transistor storage time) generally results in a very high saturation current before the eventual interruption. This high current causes heavy electrical stresses on transistor switches, which results in lower converter efficiency and reliability. Such losses establish an urgent need for a method to anticipate the impending core saturation. The anticipation initiates the turn-off of the power switch sufficiently in advance of saturation, so that by the time the switch is opened, appreciable saturation current is yet to materialize.

A published two-core transformer configuration seemed applicable for fulfilling such a need. The design was originally intended for a free-running parallel-inverter. Extending the same technique to a PWM parallel-inverter converter was investigated and experimentally demonstrated by first designing and operating a low power, low voltage PWM parallel inverter using the two-core configuration. Successful completion of this task led to the high power, high voltage design meeting all the requirements for the various loads specified in this contract.

The transformer configuration employs two identical, uncut saturable cores. By letting one core saturate before the other, an advance signal is generated with a controlled lead time for initiating the turn-off of the conducting transistor. Through such a mechanism, a complete prevention of saturation-current spike is achieved.

(2) DESIGN CRITERIA (PARALLEL INVERTER)

The transformer contains two identical cores T1 and T2, push-pull primary windings N_A and N_B , control winding N_C , and two flux-sensing windings N_D and N_E . Windings N_A , N_B , and N_C are common to both cores, while winding N_D is on T1 only, and N_E is on T2 only. The circuit loop contains N_C , N_D , and N_E is closed by resistors R_A and R_B . Generally, $N_A = N_B$, $N_D = N_E$, and $R_A = R_B$.

To analyze the steady-state performance of the two-core transformer, let both core flux start ascending from their respective negative-saturation flux levels. The five equations governing the circuit operation, based on S1 conducting, are

$$N_D \frac{d\phi_1}{dt} = e_D$$

$$N_E \frac{d\phi_2}{dt} = e_E$$

$$N_A \left(\frac{d\phi_1}{dt} + \frac{d\phi_2}{dt} \right) = E_i$$

$$N_C \left(\frac{d\phi_1}{dt} + \frac{d\phi_2}{dt} \right) = e_C$$

$$-e_{RB} + e_E + e_C - e_D + e_{RA} = 0$$

The last equation above can be simplified by neglecting e_{RA} and e_{RB} , which holds during normal converter operation when T1 and T2 are not saturated. By so doing, solutions for $d\phi_1/dt$ and $d\phi_2/dt$ can be derived as:

$$\frac{d\phi_1}{dt} = \left(\frac{E_i}{N_A} \right) \left(\frac{N_E + N_C}{N_D + N_E} \right)$$

$$\frac{d\phi_2}{dt} = \left(\frac{E_i}{N_A} \right) \left(\frac{N_E - N_C}{N_D + N_E} \right)$$

The above two equations identify the faster $d\phi_1/dt$ in relation to $d\phi_2/dt$. The positive saturation flux level of core T1 is thus reached first, with T2 still unsaturated. During the time interval when $d\phi_1/dt = 0$ and $d\phi_2/dt > 0$, a large voltage is impressed across e_{RA} and e_{RB} . Assuming $R_A = R_B$, and with $d\phi_1/dt = 0$, one has:

$$e_{RA} = e_{RB} = \frac{E_i}{2N_A} (N_Q + N_C)$$

Notice that a voltage of this amplitude exists whenever core T1 is saturated and core T2 is not. The voltage becomes an excellent anticipation signal for the pending saturation of T2. The proper design, therefore, is to utilize the leading edge of this voltage signal to initiate the turn-off of Switch S1. Taking into consideration the signal transport delay and the storage-time delay of S1, this design ensures that core T2 will not saturate within these delay intervals, thereby eliminating any saturation current associated with the two-core transformer. A detailed transformer design and discussion is presented in Appendix C.

The inductor in each output is designed to have an MMF greater than zero during steady-state operation. The output inductance L_o is therefore determined by the following constraint:

$$L_o > \frac{E_o (T_f)_{\max}}{2I_{o \min}}$$

where E_o and I_o are the dc voltage and current associated with the respective output. Using this equation, L_o for the 1kV, the +15V, the -15V, and the +5V output are designed to be 0.7H, 1.25mH, 1.25mH, and 0.53mH, respectively.

The peak flux density in the core inductor is

$$B_p = \frac{L_o P_o}{NAE_o} + \frac{E_o T_f}{2NA}$$

where N is the number of turns on the inductor, A is the cross-sectional area of the inductor core, and P_o is the output power. It is clear that the maximum B_p occurs at the maximum load and the maximum line voltage when T_f is the longest.

A high voltage 15PD114K capacitor, made by Component Research, is used for C10 across the 1kV output. This capacitor provides the least weight, and is experimentally confirmed to meet the specified ripple requirement.

The solid tantalum capacitors used in the other outputs are selected to meet the specified output ripple requirements at the cold environment when the ESR's of the capacitors are the highest. Their voltage ratings are selected to be much higher than the respective output voltage specified. Thus, in case of an inadvertent open load on any output, the abnormally high open load voltage due to peak charging of the capacitor will not cause them to fail.

APPENDIX BSUMMARY OF DC-DC CONVERTER REQUIREMENTS

<u>PERFORMANCE PARAMETERS</u>	<u>BUCK BOOST</u>	<u>SERIES SWITCHING</u>	<u>PARALLEL INVERTER</u>			
Audio Susceptibility	2.8V RMS	2.8V RMS	2.8V RMS			
Source EMI	MIL-STD-461(N3)	MIL-STD-461(N3)	MIL-STD-461(N3)			
Temperature	-25 to 80°C	-25 to 85°C	-25 to 85°C			
Input Voltage	20 to 40V	24 to 40V	24 to 40V			
Output Power	42W	40W	60W			
Efficiency at Full Load	90%	92%	85%			
Output Voltage	28V	20V	+1000V	+15V	-15V	+5V
Output Current	0 to 1.5A	0 to 2A	0.04A	0.5A	0.5A	1A
DC Output Regulation	$\pm 0.2\%$	$\pm 0.2\%$	$\pm 0.2\%$	$\pm 5\%$	$\pm 5\%$	$\pm 8\%$
Output Voltage Dynamic Regulation (Including audio-susceptibility test)	$\pm 1\%$	$\pm 1\%$	$\pm 0.5\%$	--	--	--
Output Current Regulation (including short circuit)	+5% at 120% full load	+5% at 120% full load	Overcurrent shutoff.			

APPENDIX C

GAIN OF THE PULSE MODULATION STAGE

As stated in Section 7.1.3 of the text, the proper "breaking" point for studying the SCM two-loop control system stability is at the integrator-amplifier output. In relation to Figure 27 (page 93), the gain from point A clockwise to point B has been derived in equation (27). Consequently, if one can identify the gain/phase characteristics from point B (which is the integrator output) clockwise back to point A, then a complete open loop transfer function of the SCM-controlled power processor is obtained.

Inherent in the SCM, shown in Figure 27, is the triangular ramp at the integrator-amplifier output as a result of the Loop-II rectangular inductor-voltage at the integrator input. This ramp waveform, when working in unison with the externally-generated threshold level, the DSP, and the amplified dc error due to Loop-I sensing, produces the necessary mechanism to effect the regulator duty-cycle control.

To characterize the small-signal gain/phase from point B clockwise to point A in Figure 27, one needs to identify how a disturbance at point B is propagated through the aforescribed duty-cycle control until it reaches point A. To be more general, one is interested in how the duty-cycle $d(t)$ of the power switch is being effected by a small sinusoidal disturbance at point B. The use of $d(t)$ is more versatile than voltage at point A, as the result is then applicable to all types of power-circuit configurations. In the case of Figure 27 where a buck regulator is used, the voltage at point A is simply $E_i d(t)$ when E_i is the input voltage to the power processor.

The sinusoidal-disturbance propagation is portrayed in the figure included. The figure includes both circuit implementation and waveform propagation. The switching-frequency triangular ramp and the lower-frequency disturbance are designated by v_x and v_y , respectively. The sum of v_x and v_y is compared to threshold level E_T . Using a constant - T_n duty-cycle control as an example, the intersection of $(v_x + v_y)$ with E_T marks the initiation of the T_n -interval. The length of T_n is unperturbed by v_y , as the DSP is

configured for a constant T_n . After the programmed T_n interval elapses, the length of the subsequent off time is determined by the next intersection of $(v_x + v_y)$ with E_T . Following this pattern, the duty-cycle signal $d(x)$ is illustrated accordingly.

Let the input to the pulse-modulation stage be:

$$(v_x + v_y) = A \sin \omega t$$

and let the output of the pulse-modulation stage, $d(t)$, be expressed by its Fourier series as:

$$d(t) = D + a_1 \sin \omega t + b_1 \cos \omega t \dots$$

Then, by definition, the describing function of the pulse modulation becomes:

$$F_M \triangleq \frac{(a_1^2 + b_1^2)^{1/2}}{A} e^{-j \tan^{-1}(b_1/a_1)}$$

Once a_1 and b_1 can be determined, the gain/phase of the pulse modulation are obtained.

Derivations for a_1 and b_1 are rather tedious tasks. Since the major objective of this appendix is the formulation of the physical mechanism through which $d(t)$ is being effected by $(v_x + v_y)$, the detailed mathematical derivation is not included.

For the constant- T_n pulse modulation, the describing function can be shown to be:

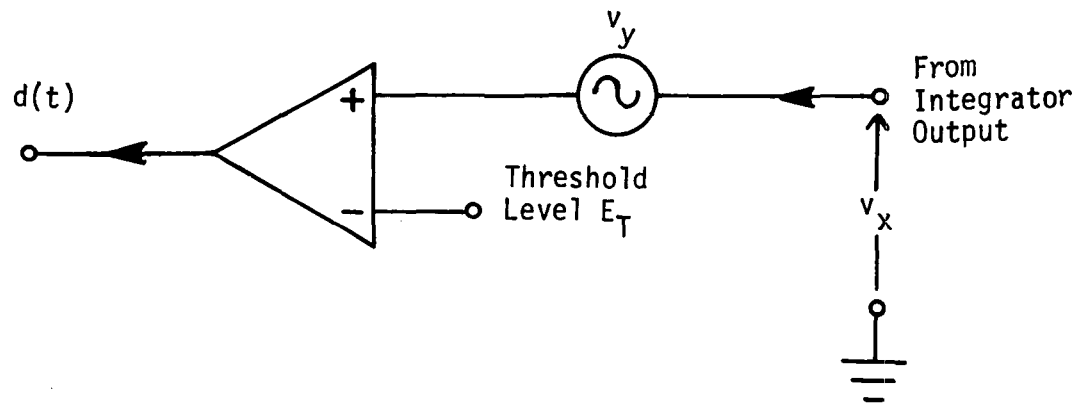
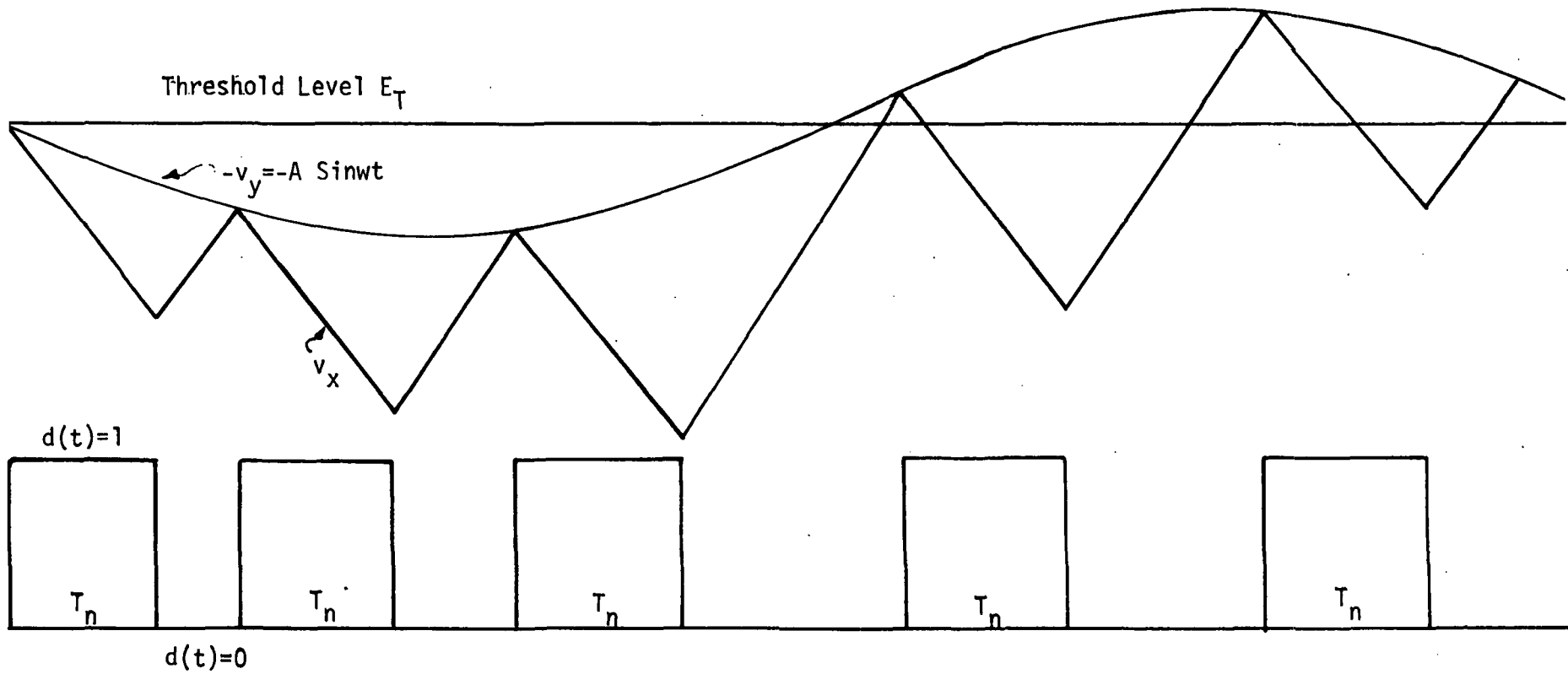
$$F_M = \frac{2D}{S_F T_n} \left[1 + \left(\frac{\omega T_n}{2} \right)^2 \right]^{1/2} e^{-j\omega T_n}$$

where D is the steady-state duty cycle without the disturbance, S_F is the slope of the steady-state integrator output ramp during the off time, and ω is the angular velocity of the sinusoidal disturbance. Based on this describing function, the gain|phase from point B to A clockwise in Figure 27 becomes:

$$K_p = \frac{2DE_i}{S_F T_n} \left[1 + \left(\frac{\omega T_n}{2} \right)^2 \right]^{1/2} e^{-j\omega T_n}$$

This value of K_p , when used in conjunction with eq. (27) on page 99 and eq. (31) on page 100, completely defines the open-loop transfer function of the SCM.

A point of particular interest is that the gain of the pulse modulation stage increases with the frequency of the disturbance signal. Realizing the validity of the equation for K_p only holds for frequencies much lower than the switching frequency due to approximations made in its derivation, the equation for K_p has been indeed verified within the signal-frequency range from essentially dc to a decade above the corner frequency of the output filter.



APPENDIX D

THE EFFECT OF TRANSIENT-RESPONSE IMPROVEMENT ON SCM STABILITY

If one neglects the effect of C_2 in Figure 27, then it has been established in Section 7.1 that the ideal autocompensation of output-filter parameters occurs when an unity NR_3/gR_4 is designed. On the other hand, it was also discussed in Section 4.4 the need for C_2 to improve the transient response. The effect of C_2 on autocompensation is thus the subject of this Appendix.

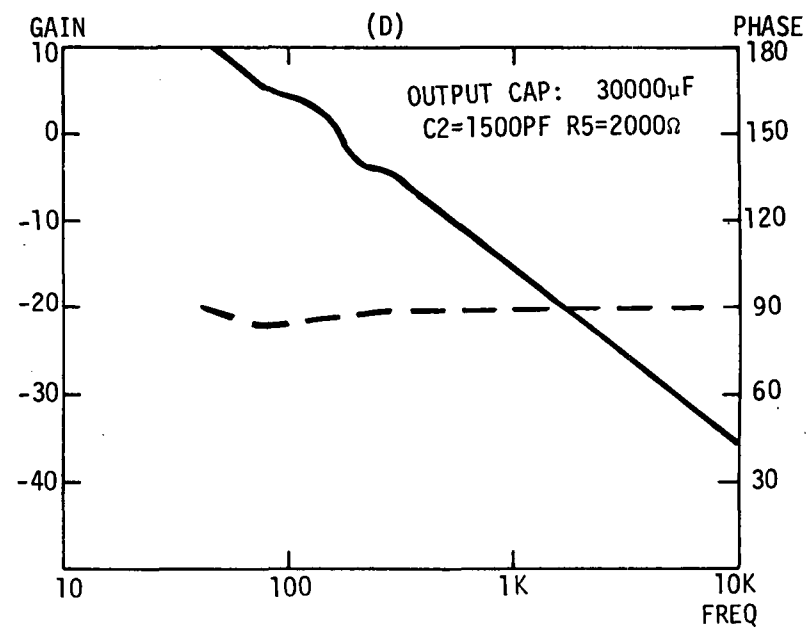
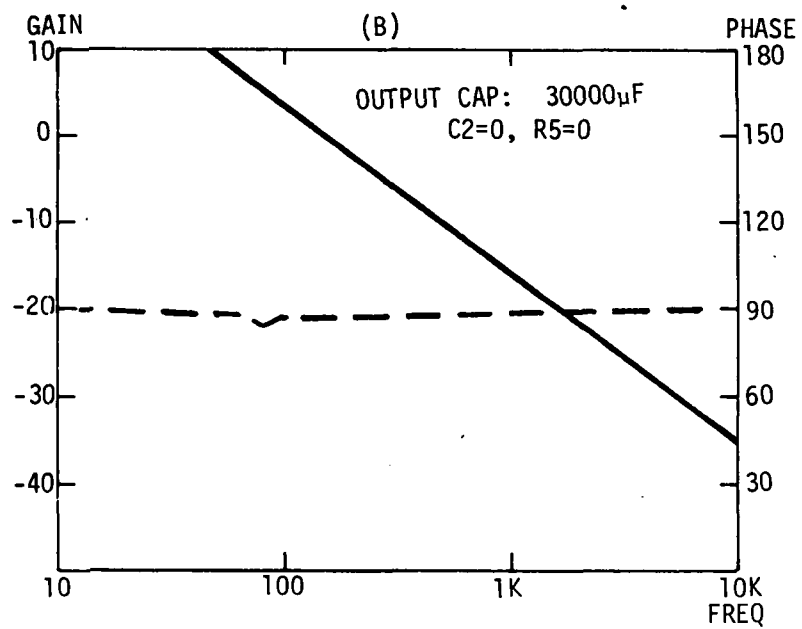
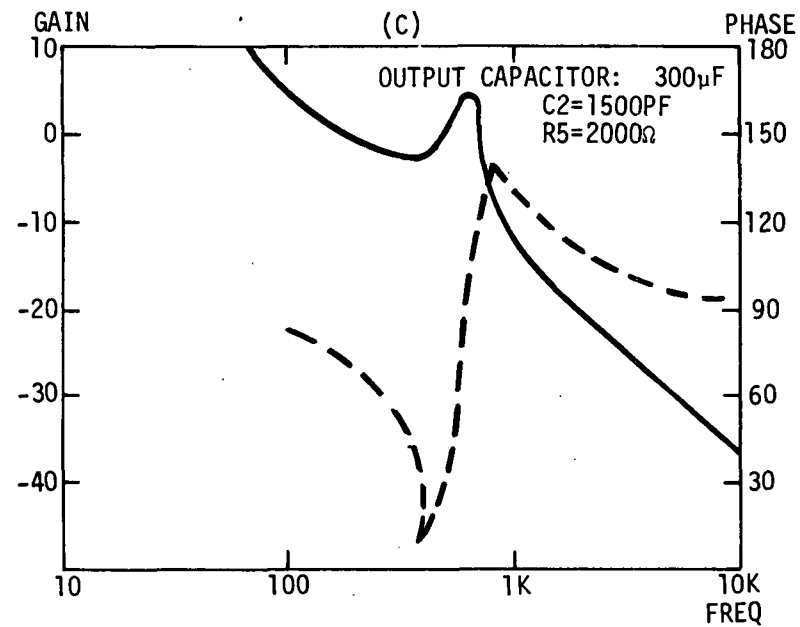
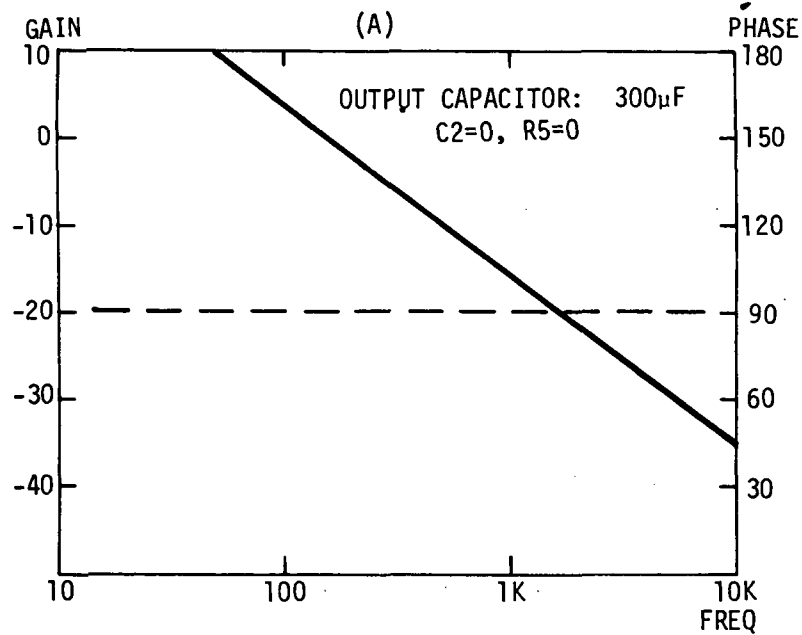
Including C_2 , the SCM open-loop transfer function from point A to B clockwise in Figure 27 was given in equation (27) of the text. Since the transfer function from point B to A clockwise has little to do with autocompensation, equation (27) alone is sufficient to assess the impact of C_2 insofar as the autocompensation is concerned. The rather complicated equation is processed by a computer program. The factor NR_3/gR_4 is set to be unity in the computer program.

Two sets of values were used for C_2 and R_5 in the computer analysis: (1) $C_2=0$, $R_5=0$, and (2) $C_2=1500\text{pF}$, and $R=2000$ ohms. For each set of C_2R_5 , output-filter capacitor C was assigned to be $300\mu\text{F}$ and $30,000\mu\text{F}$, respectively, for the benefit of evaluating the effectiveness of autocompensation upon a capacitance change of two orders of magnitude. The four sets of computer results are plotted in Figures A to D, with the values of C_2R_5 and C respectively identified.

With $C_2R_5=0$, i.e., the case of ideal autocompensation, it is seen from Figs. A and B that a change of C from $300\mu\text{F}$ to $30,000\mu\text{F}$ causes hardly any noticeable change in the phase and gain as portrayed by eq. (27). Ideal -6db/octave and 90 degree phase are obtained in either case.

With $C_2R_5=3\times 10^{-6}$ seconds, it is seen from Fig. C that at $C=300\mu\text{F}$ the gain and phase curves become bumpy, signifying the loss of the ideal autocompensation shown in Figs. A and B. However, when C is increased to $30,000\mu\text{F}$ again, the ideal autocompensation is essentially restored.

Careful examination of eq. (27) reveals the following fact: If the use of C2 and R5 does not create any stability problem for a given filter capacitor C, then any increase in C will only increase the stability margin. While such a feature cannot be compared to the absolute autocompensation in attractiveness, it nevertheless releases a power-processor designer from the concern of supplying a load that can be highly capacitive - a concern that is often expressed during the power-processor design and development stages when the nature of the load is mostly unknown.



APPENDIX E

TIME DOMAIN MODELLING AND STABILITY ANALYSIS OF AN INTEGRAL
PULSE FREQUENCY MODULATED DC TO DC POWER CONVERTER

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ABSTRACT

Using state variable representation a nonlinear, discrete-time system is derived that models the converter exactly. This system is linearized about its steady state solution, and converter stability, transient response and audio susceptibility are studied. The steady state solution of the converter is stable if and only if all the roots of the linearized system are absolutely less than unity. Excellent agreement with laboratory test data has been observed.

I. INTRODUCTION

DC to DC power converters play an important role in satellite power distribution systems, and standardization and optimization of converter design and performance are of considerable interest to the aerospace power processing industry. In order to optimize converter design and performance a thorough understanding of the converter as a system is required and one must be able to analytically predict such important converter behavior as stability, transient response and audio susceptibility (closed loop frequency response). Power converters, also called regulators, of the class considered here, employ pulse modulation for controlling the dutycycle with which a primary power source is switched to a load so that a prescribed constant load voltage is maintained. The pulse modulation process presents considerable difficulties in analyzing the behavior of these regulators by conventional frequency domain analysis techniques and many approximations in system modelling are usually required. These difficulties are apparent from recently published frequency-domain analytical results, which either limit the analytical applicability to a specific dutycycle control mode (e.g., constant frequency, constant on-time, etc.,) or assume the validity of applying linear feedback theory to nonlinear control loops [1,2].

This paper presents a new approach to the problem of converter modelling based on time domain description and analysis of pulse modulation systems [3,4]. An equivalent, nonlinear discrete time system is derived that describes the pulse modulation process and the converter behavior exactly. After linearization about the discrete time equilibrium solution (steady state), stability is readily established as a function of any arbitrary converter

parameter with the information being graphically displayed in terms of the locations of the system roots in the complex plane. Besides obtaining converter stability criteria this analysis technique also provides information on transient behavior and audio susceptibility (closed loop frequency response).

An important feature of the present approach is that it makes extensive use of a digital computer as an analysis tool, replacing many difficult and tedious analytical computations by numerical solutions and making thereby a certain degree of automation of power converter modelling and analysis possible. The developed technique promises to be a valuable tool in converter modelling and analysis. It is applied in this paper to analyze a series switched regulator (buck), but it is also applicable to other regulator configurations such as the boost and buck-boost, for example, and even to converters operating with a discontinuous inductor current. This will be described in a future paper.

II. TIME DOMAIN MODELLING

Consider the series switched regulator shown in Figure 1. The critical element of the regulator is the pulse modulator that controls the power switch Q (actually a transistor) by periodically opening and closing it in such a manner, that the output voltage e_o is maintained at some specified reference voltage E_R . By comparing the output voltage e_o with the voltage E_R an error signal is formed which is then integrated together with a voltage proportional to the derivative of e_o and an AC signal obtained from a secondary winding of the power stage inductor. Whenever the output e_c of the integrator exceeds a specified threshold E_T , the power switch closes for a predetermined fixed time T_{on} , here 20 μ sec. If upon reopening $e_c < E_T$, the switch remains open for an unknown period T_{off} until once more the condition $e_c \geq E_T$ is satisfied and the switch closes again for T_{on} seconds; if $e_c \geq E_T$ upon reopening, the switch will remain open for a minimum, fixed off-time $T_{off-min}$. This technique of

$$n = \text{Turns Ratio}$$

Formulation of State Equations

$$\frac{di}{dt} = \frac{1}{L_0} (e_i - e_o - R_o i) \quad (1)$$

$$e_o = R_5 \left(i - \frac{e_o}{R_1} \right) + v_c \quad (2)$$

$$\frac{dv_c}{dt} = \frac{1}{C_0} - \frac{e_0}{R_L C_0} \quad (3)$$

$$\frac{de_o}{dt} = e_o \left(-\frac{1}{C_o(R_5+R_L)} - \frac{R_5R_L}{L_o(R_5+R_L)} \right) \quad (4)$$

$$+ 1 \left(\frac{1}{C_o (R_5 + R_L)} - \frac{R_o R_5 R_L}{L_o (R_5 + R_L)} \right) + e_1 \left(\frac{R_5 R_L}{L_o (R_5 + R_L)} \right)$$

$$e_1 = \begin{cases} E_1 & \text{when switch Q is closed} \\ 0 & \text{when switch Q is open} \end{cases} \quad (5)$$
$$e_c = K_d E_R + \int_{t_0}^t \left\{ \frac{K_d}{R_3 C_1} (E_R - e_o) - \frac{n}{R_4 C_1} (e_i - i R_o - e_o) - \frac{C_2}{C_1} \dot{e}_o \right\} d\tau \quad (6)$$

Differentiating (6) yields

$$\dot{e}_c = \left(\frac{n}{R_4 C_1} - \frac{K_d}{R_3 C_1} \right) e_o - \frac{C_2}{C_1} \dot{e}_o + \frac{K_d}{R_3 C_1} E_R - \frac{n}{R_4 C_1} e_i + \frac{n R_o}{R_7 C_1} i \quad (7)$$

$$\bar{x} = [e_0, 1, e_c]^T \quad (8)$$
$$\bar{u}_i = [e_i, E_p]^T \quad (9)$$
$$\dot{\bar{x}} = F\bar{x} + G\bar{u} \quad (10)$$

Equivalent Nonlinear Discrete Time System

$$\bar{x}(t) = e^{(t-t_0)F} \bar{x}(t_0) + \int_{t_0}^t e^{(t-\tau)F} G u(\tau) d\tau \quad (11)$$
$$\bar{x}(t_k+T) = e^{FT} \bar{x}(t_k) + e^{FT} \left[\int_0^T e^{-Fs} ds \right] \bar{G}u(t_k) \quad (12)$$

where $\bar{u}(t) = \bar{u}(t_k) = \text{constant}$ for $t_k < t \leq t_k + T$.

Define the following matrices:

$$\phi(T) = e^{FT} \quad (13)$$

and

$$D(T) = e^{FT} \left[\int_0^T e^{-Fs} ds \right] G \quad (14)$$

The matrix $\phi(T)$ is known as the state transition matrix of the system. Equation (12) becomes now

$$\bar{x}(t_k + T) = \phi(T) \bar{x}(t_k) + D(T) \bar{u}(t_k) \quad (15)$$

The value of the input vector $\bar{u}(t_k)$ depends on the state of the switch Q at time t_k . Note that the matrices ϕ and D are only a function of the time step T which need not be constant and whose maximum permissible value is either T_{on+} or T_{off} , depending on the state of the switch at t_k .

For simple, low order systems the matrices $\phi(T)$ and $D(T)$ can often be analytically evaluated as algebraic functions of T , as is the case for the present converter system (see Appendix B). But for a general analysis applicable to a variety of converter configurations (some of possibly high order), the matrices $\phi(T)$ and $D(T)$ are evaluated numerically by a digital computer. The matrix exponential of Equation (13) is evaluated from its series representation, i.e.,

$$e^{FT} = I + FT + \frac{F^2 T^2}{2!} + \frac{F^3 T^3}{3!} + \dots \quad (16)$$

with the number of terms to be added being determined by an error criterion. Computation of $D(T)$ is then straightforward using trapezoidal or Runge-Kutta integration over the interval $[0, T]$. The computation of $\phi(T)$ and $D(T)$ is programmed as a FUNCTION SUBPROGRAM with T as a formal parameter so that $\phi(T)$ and $D(T)$ can be evaluated for any specified T .

If one cannot, or even if one does not wish to, evaluate ϕ and D in closed algebraic form, it is still useful to establish the structure of the matrices. This can be done quite easily by noting the structure of the matrices F and G and then applying the method of interpolation (Appendix B) for computing $\phi(T) = e^{FT}$ without actually performing the computations. It follows that

$$\phi = \begin{bmatrix} \phi_{11} & \phi_{12} & 0 \\ \phi_{21} & \phi_{22} & 0 \\ \phi_{31} & \phi_{32} & 1 \end{bmatrix} \quad \text{and} \quad D = \begin{bmatrix} d_{11} & 0 \\ d_{21} & 0 \\ d_{31} & d_{32} \end{bmatrix} \quad (17)$$

The zero entries in the third column of ϕ indicate that between switch times the state x_3 of the integrator does not affect the power stage variables, and the entry $\phi_{33} = 1$ identifies with the integrator. This is also clear from physical reasoning by examining the circuit diagram of Figure 1. The zeroes in

the matrix D have a similar physical interpretation with respect to the effect of the reference voltage E_R on the power stage of the regulator.

The equivalent discrete time system of the converter will now be derived. Figure 2 shows e_i as a function of time and merely serves the purpose of establishing notation regarding the time instances t_k . Note that $t_{k+1} - t_k$, for any k , is not restricted to be constant.

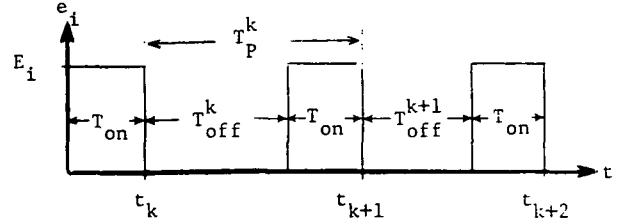


Figure 2. Input Voltage e_i as a Function of Time

The equivalent discrete time system to be given here describes the regulator behavior in terms of the time evolution of its state vector $\bar{x}$ at the discrete time instances t_k , $k = 0, 1, 2, \dots$. Defining the inputs $\bar{u}_0$ and $\bar{u}_1$ as

$$\bar{u}_0 = \begin{bmatrix} 0 \\ E_R \end{bmatrix} \quad \text{and} \quad \bar{u}_1 = \begin{bmatrix} E_i \\ E_R \end{bmatrix} \quad (18)$$

it follows from Equation (15) that

$$\bar{x}(t_{k+1}) = \phi(T_{on}) \phi(T_{off}^k) \bar{x}(t_k) + \phi(T_{on}) D(T_{off}^k) \bar{u}_0 + D(T_{on}) \bar{u}_1 \quad (19)$$

where T_{off}^k is a function of $\bar{x}(t_k)$ described implicitly by the modulator threshold condition

$$E_T = \phi_{31}(T_{off}^k) x_1(t_k) + \phi_{32}(T_{off}^k) x_2(t_k) + x_3(t_k) + d_{32}(T_{off}^k) E_R \quad (20)$$

Note that given any initial state $\bar{x}(t_0)$, Equations (19) and (20) can be used to compute recursively the state vector $\bar{x}(t_k)$ for all future time instances t_k . Therefore, these equations represent the equivalent discrete time system for the converter, describing its state at the time instances t_k exactly without any approximations. Note also that Equation (19) describes a nonlinear discrete time system because of the dependence of T_{off}^k on the state $\bar{x}(t_k)$ via Equation (20). Bringing the threshold voltage E_T to the right hand side of (20), the modulator threshold condition may be expressed in standard form as:

$$c(\bar{x}(t_k), T_{off}^k) = 0 \quad (21)$$

Equilibrium Solution

The steady state behavior or equilibrium

solution of the system (19) is of prime interest and it is defined by the condition

$$\begin{aligned}\bar{x}(t_{k+1}) &= \bar{x}(t_k) = \bar{x}^* = \text{constant for all } k \\ T_{\text{off}}^{k+1} &= T_{\text{off}}^k = T_{\text{off}}^* = \text{constant for all } k\end{aligned}\quad (22)$$

First the approximate steady state solution is computed. From duty cycle and flux conservation considerations it follows that

$$T_{\text{off}}^* \approx T_{\text{on}}(E_i - E_R)/E_R \quad (23)$$

where E_R is numerically equivalent to the regulated DC output voltage. Denoting

$$T_p^* = T_{\text{off}}^* + T_{\text{on}} \quad (24)$$

and applying (17) and (22) when expanding (19) yields for the first two rows (the third row of (19) yields no information on x_3^*),

$$\begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} \\ \phi_{21} & \phi_{22} \end{bmatrix} \begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} + \begin{bmatrix} d_{11}(T_{\text{on}}) \\ d_{21}(T_{\text{on}}) \end{bmatrix} E_i \quad (25)$$

T_p^*

which can be solved for x_1^* and x_2^* since T_p^* is approximately known. Thus,

$$\begin{bmatrix} x_1^* \\ x_2^* \end{bmatrix} = E_i \begin{bmatrix} 1-\phi_{11} & -\phi_{12} \\ -\phi_{21} & 1-\phi_{22} \end{bmatrix}^{-1} \begin{bmatrix} d_{11}(T_{\text{on}}) \\ d_{21}(T_{\text{on}}) \end{bmatrix} \quad (26)$$

T_p^*

The third state x_3^* is determined from the threshold condition (20) as:

$$x_3^* = E_T - \phi_{31}(T_{\text{off}}^*) x_1^* - \phi_{32}(T_{\text{off}}^*) x_2^* - d_{32}(T_{\text{off}}^*) E_R \quad (27)$$

The steady state solution $\bar{x}^*$ determined by this method is not exact because the power circuit is not completely lossless so that the duty cycle relationship of (23) is only an approximation, but a very good one. How well this $\bar{x}^*$ approximates the true equilibrium solution can be determined by checking how closely $\bar{x}_k$ and $\bar{x}_{k+1}$ match when using (19) for propagating the state through one cycle starting with $\bar{x}_k = \bar{x}^*$. The best method for determining the exact steady state is to determine the exact T_{off}^* by iterative linearization (Newton's method) on the cycle to cycle matching condition for the third state (which is the integrator output and directly controls the threshold condition). The iterative process is started with the above computed approximate steady state values and thus converges usually very fast. More details of this procedure are described next.

Define the system state when the power switch

turns on as:

$$\bar{z}_k \triangleq \bar{x}(t_k + T_{\text{off}}^k) \quad (28)$$

and clearly

$$z_3(t_k) = E_T \quad \text{for all } k = 0, 1, 2, \dots \quad (29)$$

In the steady state one has:

$$\begin{bmatrix} z_1^* \\ z_2^* \\ E_T \end{bmatrix} = \begin{bmatrix} \phi_{11} & \phi_{12} & 0 \\ \phi_{21} & \phi_{22} & 0 \\ \phi_{31} & \phi_{32} & 1 \end{bmatrix} \begin{bmatrix} x_1^* \\ x_2^* \\ x_3^* \end{bmatrix} + \begin{bmatrix} d_{11} & 0 \\ d_{21} & 0 \\ d_{31} & d_{32} \end{bmatrix} \begin{bmatrix} 0 \\ E_R \end{bmatrix} \quad (30)$$

T_{off}^* T_{off}^*

Clearly, if $\bar{x}^*$ and T_{off}^* are the exact steady state values, then one must satisfy the state matching condition:

$$\begin{aligned}S_{\text{match}} &= x_3^* - [\phi_{31}(T_{\text{on}}) z_1^* + \phi_{32}(T_{\text{on}}) z_2^* + E_T + d_{31}(T_{\text{on}}) E_i \\ &\quad + d_{32}(T_{\text{on}}) E_R] = 0\end{aligned}\quad (31)$$

since the square bracketed term should equal x_3^* . Note now that via Equations (26), (27) and (30), the function S_{match} is really only a function of T_{off}^* , and one wishes to determine T_{off}^* such that

$$S_{\text{match}}(T_{\text{off}}^*) = 0 \quad (32)$$

Iterative linearization (Newton's method [11]) may now be applied to (32) to determine the exact value for T_{off}^* . The entire procedure is performed by the computer with the required partial derivative $\partial S_{\text{match}} / \partial T_{\text{off}}^*$ being evaluated numerically. Convergence from the approximate steady state to the exact steady state is usually within 1-3 iterations.

Note that the difference between $\bar{x}^*$ and $\bar{z}^*$ denotes the peak-to-peak steady state ripple, provided the inductor current i and output voltage e_o are in phase. This is usually the case, unless the series equivalent resistance R_s of the capacitor C_o is equal to zero. Note that x_1^* denotes the maximum value, and z_1^* the minimum value, of the limit cycle of the regulated output e_o .

III. STABILITY ANALYSIS

Regarding stability of the discrete time non-linear system (19)-(20) one may now consider two approaches: (1) Determine stability-in-the-large*, and (2) determine stability of the equilibrium solution.

*Given any initial state $\bar{x}(t_0)$, show that it will converge to the equilibrium solution.

The task of analytically determining stability-in-the-large appears to be a difficult one. Initial attempts of relating stability-in-the-large to the contraction mapping/fixed point theorem [7] approach to solving Equations (19) and (20) have failed. So have attempts of using the second method of Liapunov [3,8]. But hope for success at some future time has not been entirely dispelled so that further research in this area appears to be indicated. Establishing stability-in-the-large is basically equivalent to solving the converter start-up problem. This can, however, be studied using a digital simulation based on Equations (19) and (20), since usually a fixed start-up procedure is followed, i.e., convergence to the equilibrium solution from only a well defined set of initial states need be considered and not from any state in the entire state space.

Of more importance at the moment is to establish stability of the equilibrium solution, which will be accomplished by linearization. The linearized system can also be used to study small signal audio susceptibility and transient behavior of the converter. It should be kept in mind, however, that the results thus obtained will not be valid for arbitrarily large displacements of the system from its equilibrium, and that when certain system parameters are varied such that instability of the equilibrium is approached, the region to which the linearized system applies may become small.

The Linearized System

The nonlinear, discrete time system described by Equations (19) and (20) will now be linearized about its steady state equilibrium solution $\bar{x}^*$, and the nominal DC supply voltage E_1^* . Denoting

$$\delta \bar{x}(t_k) = \bar{x}(t_k) - \bar{x}^* \quad \text{and} \quad \delta E_1(t_k + T_{\text{off}}^*) = E_1(t_k + T_{\text{off}}^*) - E_1^* \quad (33)$$

it follows that

$$\begin{aligned} \delta \bar{x}(t_{k+1}) = & \left\{ \phi(T_{\text{on}}) \frac{\partial}{\partial \bar{x}} \left[\phi(T_{\text{off}}^k) \bar{x}(t_k) + D(T_{\text{off}}^k) \bar{u}_0 \right] \right\} \delta \bar{x}(t_k) \\ & + \left\{ \frac{\partial}{\partial E_1} \left[D(T_{\text{on}}) \bar{u}_1 \right] \right\} \delta E_1(t_k + T_{\text{off}}^*) \end{aligned} \quad (34)$$

where it is important to note that T_{off}^k is a function of $\bar{x}_k$ via the threshold condition (20), i.e., $\zeta(\bar{x}(t_k), T_{\text{off}}^k) = 0$.

In the previous developments it had been tacitly assumed that $E_1 = E_1^*$ = constant for all time. This is not necessarily so and the nonlinear discrete time system (19)-(20) is also an exact description of the converter if E_1 is time-varying, provided E_1 remains constant over any T_{on} period. To assume a time-varying E_1 composed of the nominal DC value E_1^* plus a small superimposed AC component δE_1 , is a useful

concept when investigating audio susceptibility of the converter and is the main reason why it is included here in the derivation of the linearized system.

Denoting the first curly bracketed term in (34) by Ψ , a constant 3×3 matrix, and the second curly bracketed term by Γ , a constant 3-dimensional column vector, Equation (34) can now be written as

$$\delta \bar{x}(t_{k+1}) = \Psi \delta \bar{x}(t_k) + \Gamma \delta E_1(t_k + T_{\text{off}}^*) \quad (35)$$

and it represents the sought linearized system. The matrix Ψ and the column vector Γ remain to be evaluated, however.

By definition,

$$\Psi = \phi(T_{\text{on}}) \frac{\partial}{\partial \bar{x}} \left[\phi(T_{\text{off}}^k) \bar{x}(t_k) + D(T_{\text{off}}^k) \bar{u}_0 \right] \bigg|_{\bar{x}^*} \quad (36)$$

To evaluate the partial derivatives of the square bracketed term analytically turns out to be possible but a very tedious task and it is much easier evaluated numerically by using difference quotients.

Denote the continuous function $\bar{F}(\bar{x})$ by

$$\bar{F}(\bar{x}) = \phi(T_{\text{off}}^k) \bar{x}(t_k) + D(T_{\text{off}}^k) \bar{u}_0 \quad (37)$$

and for sufficiently small Δx_i , $i = 1, 2, 3$, one has that

$$\frac{\partial \bar{F}}{\partial \bar{x}} \bigg|_{\bar{x}^*} \approx \begin{bmatrix} \frac{f_1(x_1^* + \Delta x_1) - f_1(x_1^*)}{\Delta x_1} & \dots & \frac{f_1(x_3^* + \Delta x_3) - f_1(x_3^*)}{\Delta x_3} \\ \vdots & & \vdots \\ \frac{f_3(x_1^* + \Delta x_1) - f_3(x_1^*)}{\Delta x_1} & \dots & \frac{f_3(x_3^* + \Delta x_3) - f_3(x_3^*)}{\Delta x_3} \end{bmatrix} \quad (38)$$

In order to evaluate (38) one must first determine by how much T_{off} changes due to a change Δx_j ,

$j = 1, 2, 3$, and then use the new T_{off} to compute the $f_i(x_j + \Delta x_j)$, $i, j = 1, 2, 3$. The threshold condition

$$\zeta(\bar{x}, T_{\text{off}}) = 0 \quad (39)$$

is used to determine the change in T_{off} due to a change in $\bar{x}$. Iterative linearization (Newton's method) is used to determine the new T_{off} that satisfies $\zeta = 0$ after $\bar{x}$ has been perturbed by Δx_j , $j = 1, 2, 3$. The only problem with numerical differentiation is to select the appropriate increments Δx_j . At the present the increments are taken as 1% of the value of the independent variable, i.e.,

$$\Delta x_j = 0.01 |x_j^*| \quad (40)$$

Some experimentation with the increment size is advisable, since the accuracy of the partial derivatives depends on it. For instance, if the function varies rapidly, a very small increment is clearly required. On the other hand, if the increment is chosen needlessly too small, then the accuracy degrades because of numerical problems, since in the limit a difference quotient assumes numerically the value 0/0. Studies on the increment size and its effect on the results have also physically significant implications. If the linearized system shows high sensitivity to increment size, then this points out that the nonlinear system changes its behavior rather rapidly as it moves away from its equilibrium point, and the results obtained for the linearized system are only valid for very small perturbations about the equilibrium. A computationally slightly more complex, but perhaps also more accurate way of computing a derivative numerically is to use the following approximation,

$$\left. \frac{\partial f}{\partial x} \right|_x = \frac{f(x^* + \Delta x) - f(x^* - \Delta x)}{2\Delta x} \quad (41)$$

which can also detect discontinuities.

The 3 x 1 matrix Γ can be evaluated analytically, and by inspection of (34) it follows that:

$$\Gamma = \begin{bmatrix} d_{11}(T_{on}) \\ d_{21}(T_{on}) \\ d_{31}(T_{on}) \end{bmatrix} \quad (42)$$

since E_1 enters linearly into the system.

Stability of the Linearized System

To assess stability of the steady state solution one now examines the stability of the linearized system (35), restated here for convenience:

$$\delta \bar{x}(t_{k+1}) = \Psi \delta \bar{x}(t_k) + \Gamma \delta E_1(t_k + T_{off}^*) \quad (43)$$

This system is stable if and only if all the eigenvalues λ_i of Ψ are absolutely less than unity, that is,

$$|\lambda_i(\Psi)| < 1, \quad i=1,2,3 \quad (44)$$

The eigenvalues of Ψ are evaluated by a digital computer and changes in the eigenvalues as a function of system parameters can be plotted in the complex plane. The locations of the eigenvalues, which are the roots of the system, do not only indicate stability, but also govern the transient behavior of the converter after a disturbance has displaced it from its equilibrium. The existing relationships between root locations inside the unit circle and corresponding system response times and damping are well known results from z-transform analysis of linear discrete time systems [9,10].

Stability Results

A digital computer program has been written that computes the equilibrium solution x^* , evaluates the

matrix Ψ , and computes the eigenvalues λ_i , $i = 1,2,3$.

For nominal converter parameters as listed in Table 1 one expects to obtain three real and positive eigenvalues less than unity, since it is known from actual converter breadboard tests that this system is stable and that after a disturbance the resulting transient decays in a nonoscillatory manner. This was the case as can be ascertained from the computer results shown in Table 2. Note that one root (eigenvalue) is for all practical purposes equal to zero. This is because the incremental integrator output voltage δe_c can be shown to be a linear combination of the incremental inductor current δi and the incremental output voltage δe_o , provided the inductor series resistance R_o equals zero, which is almost the case here. The zero eigenvalue should, therefore, cause no concern: it does not affect stability, being clearly less than unity, and results will focus here mainly on the two other, nonzero eigenvalues.

Table 1. Nominal Circuit Parameter Values

Symbol	Parameter	Units	Value
E_1	Supply Voltage	volts	30
E_R	Reference (Desired Output) Voltage	volts	20
E_T	Integrator Threshold	volts	8
R_o	Inductor Series Resistance	ohms	0.015
R_1	Part of Output Voltage Divider	ohms	28.7K
R_2	Part of Output Voltage Divider	ohms	13.5K
R_3	Op-amp DC Input Resistor	ohms	10K
R_4	Op-amp AC Input Resistor	ohms	100K
R_5	Series-equivalent Resistance of C_o	ohms	0.077
R_L	Load	ohms	10.
C_o	Output Filter Capacitor	μF	300
C_1	Op-amp Feedback Capacitor	pF	2200
C_2	Lead Compensation Capacitor	μF	0.022
L_o	Output Filter Inductor/Transformer	μH	250
n	Transformer Turns Ratio n_2/n_1	--	0.65
T_{on}	On-Time	μs	20
$T_{off-min}$	Minimum Off-Time	μs	5

Table 2. Computer Stability Results

```

E1= 3.0000E+01 (volts)
TON= 2.0000E-05 TOff= 9.4551E-06 1P= 2.4435E-05 (sec)
X= 2.0033E+01 2.3988E+00 6.8015E+00 = X* (volts, amps, volts)
Z= 1.9972E+01 1.6009E+00 8.0000E+00 = Z*
Y= 6.0989E-02 7.9777E-01 -1.1985E+00 = Y* - Z* (Peak-Peak Ripple)

PS1=
9.7102E-01 6.6839E-02 9.3672E-02
-1.4513E-01 7.9768E-01 5.9146E-01
-3.2488E-02 -5.3217E-01 -4.0041E-01

LAMBDA=
4.1176E-01 0. 9.5634E-01 0. 1.9027E-15 0.

```

The developed computer program is now used to compute the roots of the linearized system as a function of important system parameters, thereby yielding valuable design information on system stability and transient behavior. Critical parameters are the AC loop gain embodied in R_4 or n_2 , the DC loop gain embodied in R_3 , and the lead capacitor C_2 . The motion of the roots can be plotted in the complex plane, and as long as they remain inside the unit circle, the system is stable. The system is at the verge of instability for those parameter values for which the roots are just crossing the unit circle, and it is unstable when the roots are outside the unit circle. Figures 3 through 5 show some of the root locus plots that were obtained. Figure 4, for example, predicts that without the AC loop, the converter will become unstable as C_2 is decreased below 600 pF. It also shows that without the AC loop no complex roots are obtained which considerably restricts the ability to shape response time and damping of the converter transients. This clearly demonstrates that the main advantage of the AC loop is to provide an additional degree of design freedom for adjusting the transient behavior of the converter independent of the output filter parameters. Note that the present root locus plots are not exactly equivalent to those usually encountered in control systems design, since here no "zeros" exist because the system has not been characterized by a transfer function. From the results of the stability analysis the following conclusions could be drawn:

- The capacitor C_2 provides lead information and is critical for stability.
- The AC loop also acts as a stabilizing lead, but is less critical in the presence of C_2 compensation. Its advantage is that it can adjust the transient response independent of the output filter parameters L_o , C_o and the load R_L .
- With $C_2 = 0$, the system can be stabilized by the AC loop alone, but it will be oscillatory and only marginally stable.
- Without the AC loop, the system can be stabilized by C_2 alone very well. The AC loop plays therefore a less important role in stabilizing the system.
- The present operating point of the converter is good, but its transient response can be improved (speeded up) by lowering C_2 from $C_2 = 22,000$ pF to $C_2 = 5,000$ pF. As can be seen in Figure 3, this creates a pair of complex roots with a 0.707 damping ratio and a higher natural frequency as before.
- Near instability the system is extremely sensitive to the series equivalent resistance R_5 of the capacitor C_o .

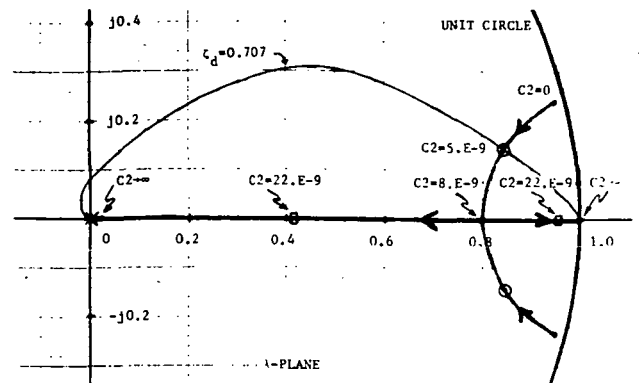


Figure 3. Root Loci for Linearized System: Effect of Lead Capacitor C_2 with Nominal AC Loop

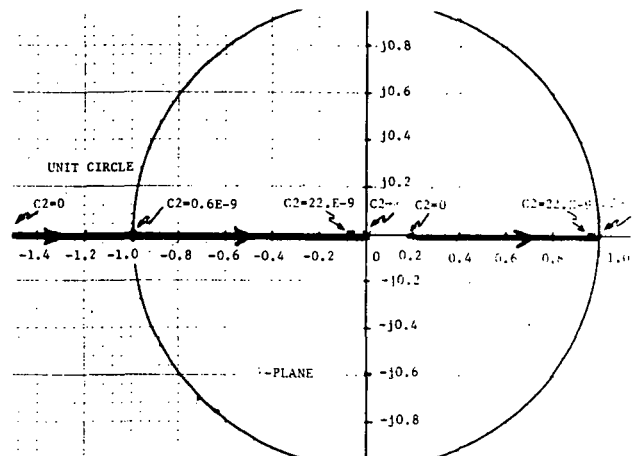


Figure 4. Root Loci for Linearized System: Effect of Lead Capacitor C_2 with AC Loop Open

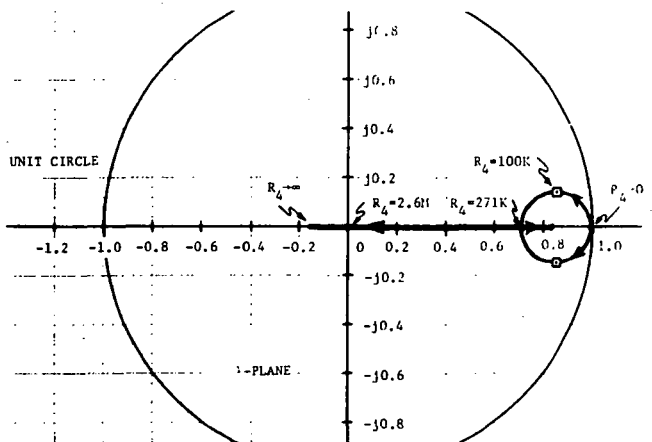


Figure 5. Root Loci of Linearized System: Effect of AC Loop When $C_2 = 5000$ pF

The analytically predicted results on stability and transient behavior were then compared with laboratory results obtained from an actual breadboard model of the converter and good agreement was observed. Reducing the capacitor C_2 from 22,000 pF to 5000 pF resulted, as predicted, in a faster

transient response exhibiting an oscillatory overshoot of 5% that is characteristic for a damping ratio of $\zeta_d = 0.707$. When C_2 was reduced further to $C_2 = 0$, the system remained stable, but its transient response became now quite oscillatory with very little damping, just as expected in accordance with the corresponding root locations at $C_2 = 0$ as shown in Figure 3. When C_2 was reduced from 22,000 pF toward zero with the AC loop open, the behavior of the converter could be directly correlated with the corresponding root locations in Figure 4. The only observed discrepancy was that the breadboard model became unstable for values of $C_2 \leq 1000$ pF while the analysis predicted instability to occur only at $C_2 \leq 600$ pF, a relatively minor inconsistency. Near instability the region about the steady state to which the linearized system applies may be quite small and any otherwise insignificant disturbance may cause the system to leave this region and become unstable. Variations in the AC loop gain when C_2 was held constant at 5000 pF resulted in a converter behavior that also correlated well with the corresponding root locations in Figure 5.

IV. AUDIO SUSCEPTIBILITY

It is of interest to examine how sinusoidal oscillations of the supply voltage E_1 about its nominal DC value affect the regulated output voltage e_o in the steady state. The z-transform method can be applied to derive a frequency domain transfer function since in the steady state the cycle period $T_p^* = T_{on} + T_{off}^*$ is constant. Furthermore, the amplitude of the supply voltage oscillations is constrained to be small and therefore the linearized system model of Equation (43) applies. Taking the z-transform of the vector difference equation (43) and noting that by definition $e_o = x_1$, one obtains

$$\delta E_o(z) = H(zI - \Psi)^{-1} \Gamma e^{sT_{off}^*} \delta E_1(z) \quad (45)$$

where

$$H = [1, 0, 0] \quad (46)$$

After setting $z = e^{j\omega T_p^*}$, the frequency domain transfer function $G = \delta E_o / \delta E_1$ is given by

$$G(j\omega) = H(Ie^{j\omega T_p^*} - \Psi)^{-1} \Gamma e^{j\omega T_{off}^*}, \quad 0 \leq \omega T_p^* \leq \pi \quad (47)$$

which by virtue of the sampling theorem applies up to one-half the sampling frequency, i.e., up to $\omega T_p^* = \pi$. For the present converter this means up to 16.6 KHz which comprises the entire frequency band of interest. Note that the purely multiplicative factor $e^{j\omega T_{off}^*}$ contributes only to the phase information of $G(j\omega)$ and can be ignored for amplitude computations.

This is also clear from physical reasoning since the term merely reflects the time shift of the sinusoidal input $\delta E_1(t)$ by T_{off} relative to the discrete reference times t_k , see Figure 2.

The transfer function $G(j\omega)$ of (47) can be easily evaluated at any desired ω by a digital computer. The results are shown in Figure 6 in comparison with laboratory test data obtained from a breadboard model of the converter and agreement is quite good. Between 50 Hz and 1.2 KHz the measured audio susceptibility differs from the computed values by only 1-2 db out of a total attenuation of about -42 db, while at higher frequencies a maximum deviation of up to 3.4 db can be observed, amounting to a maximum error of 8%. As can be seen, the computed frequency response predicts less attenuation than actually measured. This is most likely caused by the fact that the mathematical system model cannot be a perfect description of the actual physical system which apparently is slightly more lossy than predicted. The mathematical description modelled the power transistor and the diode as ideal switches, while in reality some losses are incurred in these devices; also, due to transistor storage time, the switch is not perfect. It should also be remembered that at higher frequencies the assumption that E_1 is constant over the fixed time period $T_{on} = 20$ μ sec becomes a poorer approximation; this is however expected to contribute only a minor error since the effect tends to average out.

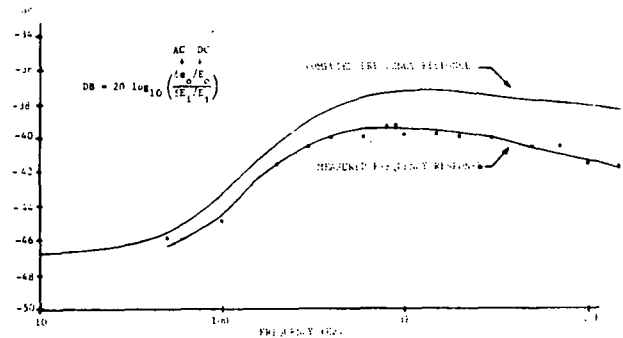


Figure 6. Audio Susceptibility of Converter

The measured frequency response data was obtained by feeding the regulator output voltage into an harmonic wave analyzer. This can also contribute to the discrepancy observed. For it will lead to slightly different results than obtained from computing the amplitude of the envelope of e_o , whenever the upper and lower envelopes of e_o are not exactly in-phase, as was observed here over several frequency ranges.

V. TRANSIENTS CAUSED BY SUPPLY VOLTAGE STEP CHANGES

Of great interest is the transient behavior of the converter after a step change in the supply voltage E_1 . The linearized system remains valid for transient analysis, since the converter continues

to operate about its steady state equilibrium. The transient resulting from a step change of E_i from, say 30 to 40 volts, should be looked at as a transient of the $E_i = 40$ volt system when displaced from its equilibrium. The closed loop root locations in the complex plane govern the decay of the transient with respect to damping and rapidity of response [9], but the peak overshoot observed after supply voltage switching depends on the "initial state", which is the state of the converter when the supply voltage step change first becomes effective. For the present converter note that the peak of the first cycle after switching E_i is completely independent of the controller (dashed box of Figure 1) and only depends on the output filter and load. This first peak can be readily computed by judiciously applying Equation (19) as follows. Using the old equilibrium $\bar{x}^*$, first compute the corresponding state $\bar{z}^*$ at $t_{k-1} + T_{off}^*$ (see Figure 2):

$$\begin{bmatrix} z_1^* \\ z_2^* \\ z_3^* = E_T \end{bmatrix} = \phi(T_{off}^*) \begin{bmatrix} x_1^* \\ x_2^* \\ x_3^* \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ d_{32}(T_{off}^*)E_R \end{bmatrix} \quad (48)$$

Assuming that the supply voltage switch and corresponding change in T_{on} occurred at some time t between t_{k-1} and $t_{k-1} + T_{off}^*$, it follows that the peak of the first cycle at t_k is given by

$$\begin{bmatrix} x_1^o(t_k) \\ x_2^o(t_k) \\ x_3^o(t_k) \end{bmatrix} = \phi(T_{on}^{new}) \begin{bmatrix} z_1^* \\ z_2^* \\ E_T \end{bmatrix} + \begin{bmatrix} d_{11} \\ d_{21} \\ d_{31} \end{bmatrix} E_i^{new} + \begin{bmatrix} 0 \\ 0 \\ d_{32}(T_{on}^{new}) \end{bmatrix} E_R \quad (49)$$

This first peak, $\bar{x}_k^o$, after switching now forms the initial state for the new system and the convergence from $\bar{x}_k^o$ to the new steady state equilibrium is governed by the linearized system (35), with the linearization having been performed about the new equilibrium, of course. Thus, defining the incremental initial state by

$$\delta \bar{x}(t_0) \triangleq \bar{x}^o(t_k) - \bar{x}_{new}^* \quad (50)$$

the time history of the transient is defined by the discrete time response of the linear system

$$\delta \bar{x}(t_{k+1}) = \psi \delta \bar{x}(t_k) \quad (51)$$

starting with the initial state $\delta \bar{x}(t_0)$ given in (50).

Investigating the behavior of the transient is now done best by propagating Equation (51) over a few cycles until the actual peak response has been observed. From then on the decay of the transient

is solely determined by the roots. Propagation of (51) is done best by a digital computer, although the low order of the present system makes it possible to perform the required computations with a pocket size electronic calculator. Obtained results were compared with laboratory data from a breadboard model, and good agreement was observed.

VI. CONCLUSIONS

A time domain approach based on state space techniques has been applied to modelling and analysis of an integral pulse frequency modulated DC to DC power converter. An equivalent, nonlinear discrete time system was derived that describes the converter without approximations. This system was linearized about its equilibrium solution, which is the steady state of the converter, and from the obtained linear discrete time system, converter stability, transient response and audio susceptibility could readily be established. A key feature of this approach is that it makes extensive use of a digital computer as an analysis tool, thereby facilitating a certain degree of automation in power converter modelling and analysis. The analytically predicted results were compared with laboratory test data obtained from an actual breadboard model of the converter and very good agreement was observed.

The approach to converter modelling and analysis presented here has with very good results also been applied to a pulse width modulated buck regulator (the converter of Figure 1 with a different dutycycle control mode). Furthermore, the concept of system modelling by a state transition matrix was used in digital simulation of converters, resulting in significantly faster program execution times. Currently the approach is being successfully applied to other power converter configurations, such as boost and buck boost for instance, and to converters operating with a discontinuous inductor current. The results of this research will be presented in a future paper.

The analysis approach developed in this paper can be generalized and applied to a large variety of converters and it should prove to be a very valuable tool in power converter modelling and analysis in the future.

APPENDIX A

Entries of Matrices F and G

In expanded form Equation (10) can be written as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \\ \dot{x}_3 \end{bmatrix} = \begin{bmatrix} f_{11} & f_{12} & 0 \\ f_{21} & f_{22} & 0 \\ f_{31} & f_{32} & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} g_{11} & 0 \\ g_{21} & 0 \\ g_{31} & g_{32} \end{bmatrix} \begin{bmatrix} e_i \\ E_R \end{bmatrix} \quad (A-1)$$

where

$$f_{11} = -\frac{1}{C_o(R_5+R_L)} - \frac{R_5 R_L}{L_o(R_5+R_L)}$$

$$f_{12} = \frac{R_L}{C_o(R_5+R_L)} - \frac{R_o R_5 R_L}{L_o(R_5+R_L)} \quad (A-2)$$

$$f_{21} = -\frac{1}{L_o}, \quad f_{22} = -\frac{R_o}{L_o}$$

$$f_{31} = \frac{n}{R_4 C_1} - \frac{K_d}{R_3 C_1} + \frac{C_2}{C_1 C_o(R_5+R_L)} + \frac{C_2 R_5 R_L}{C_1 L_o(R_5+R_L)}$$

$$f_{32} = \frac{C_2 R_o R_5 R_L}{C_1 L_o(R_5+R_L)} - \frac{R_L C_2}{C_1 C_o(R_5+R_L)} + \frac{R_o n}{R_4 C_1}$$

$$g_{11} = \frac{R_5 R_L}{L_o(R_5+R_L)}, \quad g_{21} = \frac{1}{L_o} \quad (A-3)$$

$$g_{31} = -\frac{n}{R_4 C_1} - \frac{C_2 R_5 R_L}{C_1 L_o(R_5+R_L)}$$

$$g_{32} = \frac{K_d}{R_3 C_1}$$

APPENDIX B

Analytic Determination of the State Transition Matrix $\phi(T)$

The Cayley-Hamilton theorem [5] is applied to determine $\phi(T) = e^{FT}$; this technique is also known as the method of interpolation [6]. Thus, since F is a 3×3 matrix,

$$\phi(T) \triangleq e^{FT} = \gamma_o I + \gamma_1 F + \gamma_2 F^2 \quad (B-1)$$

where the γ_i are scalar functions of T which must be determined. To do this the eigenvalues λ of F are needed, which are the roots of $\det(F-\lambda I) = 0$. Hence,

$$\lambda[\lambda^2 - (f_{11}+f_{22})\lambda - f_{12}f_{21} + f_{11}f_{22}] = 0$$

yields

$$\lambda_{1,2} = \frac{f_{11}+f_{22}}{2} \pm j \sqrt{f_{11}f_{22} - f_{12}f_{21} - (f_{11}+f_{22})^2/4},$$

$$\lambda_3 = 0 \quad (B-2)$$

which is rewritten as

$$\lambda_1 = -\alpha + j\beta, \quad \lambda_2 = -\alpha - j\beta, \quad \lambda_3 = 0 \quad (B-3)$$

Substituting λ 's for F in (B-1) yields

$$e^{(-\alpha+j\beta)T} = \gamma_o + \gamma_1(-\alpha+j\beta) + \gamma_2(-\alpha+j\beta)^2$$

$$e^{(-\alpha-j\beta)T} = \gamma_o + \gamma_1(-\alpha-j\beta) + \gamma_2(-\alpha-j\beta)^2 \quad (B-4)$$

$$1 = \gamma_o$$

Solving these equations for the γ 's yields

$$\gamma_o = 1 \quad (B-5)$$

$$\gamma_1 = \frac{2\alpha}{\alpha^2+\beta^2} \left\{ 1 - e^{-\alpha T} \left[\frac{\alpha^2-\beta^2}{2\alpha\beta} \sin\beta T + \cos\beta T \right] \right\} \quad (B-6)$$

and

$$\gamma_2 = \frac{1}{\alpha^2+\beta^2} \left\{ 1 - e^{-\alpha T} \left[\frac{\alpha}{\beta} \sin\beta T + \cos\beta T \right] \right\} \quad (B-7)$$

Thus, (B-1) represents a closed form expression of $\phi(T)$.

Determination of the Matrix $D(T)$

The only nontrivial computation required is the evaluation of the matrix integral, see Equation (14). From (B-1) it follows that

$$\int_0^T e^{-sF} ds = TI + F \int_0^T \gamma_1(-s) ds + F^2 \int_0^T \gamma_2(-s) ds \quad (B-8)$$

$$= TI + F\xi_1(T) + F^2\xi_2(T)$$

By direct evaluation

$$\xi_1(T) = \frac{2\alpha}{\alpha^2+\beta^2} \left\{ T - \frac{1}{\alpha^2+\beta^2} \left[e^{\alpha T} (\alpha \cos\beta T + \beta \sin\beta T) - \alpha \right] \right. \quad (B-9)$$

$$\left. + \frac{\alpha^2-\beta^2}{2\alpha\beta(\alpha^2+\beta^2)} \left[e^{\alpha T} (\alpha \sin\beta T - \beta \cos\beta T) + \beta \right] \right\}$$

$$\xi_2(T) = \frac{1}{\alpha^2+\beta^2} \left\{ T - \frac{1}{\alpha^2+\beta^2} \left[e^{\alpha T} (\alpha \cos\beta T + \beta \sin\beta T) - \alpha \right] \right. \quad (B-10)$$

$$\left. + \frac{\alpha}{\beta(\alpha^2+\beta^2)} \left[e^{\alpha T} (\alpha \sin\beta T - \beta \cos\beta T) + \beta \right] \right\}$$

Then,

$$D(T) = \phi(T) [TI + F\xi_1(T) + F^2\xi_2(T)] G \quad (B-11)$$

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APPENDIX F

COST EFFECTIVE TIME-DOMAIN SIMULATION

Equations (15) of Appendix E, together with the closed-form expressions in eqs. (B-1) to (B-11) of Appendix E, serve as a good starting point for the simulation of regulator performances. From Figure 27, it is apparent that the system has three states: the output voltage, the current through L_o , and the output voltage of the integrator amplifier.

Note that with $T = \text{constant}$, $\phi(T)$ and $D(T)$ of eqs. (B-1) to (B-11) of Appendix E become constant matrices which need be computed only once. This can be done for the constant converter "on" period with $T = T_n$. Defining

$$\phi(T_n) = \phi_n = \text{constant and } D(T_n) = D_n = \text{constant},$$

Equation (15) of Appendix E becomes

$$\bar{x}(t_k + T_n) = \phi_n \bar{x}(t_k) + D_n \bar{u}(t_k)$$

As for the "off" period, T_f is generally not constant, being a variable determined by input/output conditions. Using the closed-form expressions for $\phi(T)$ and $D(T)$, T_f can be solved for implicitly or by linearization about a nominal value. Let

$$T_f^* = \text{nominal value of } T_f,$$

then, one can define and precompute the constant matrices

$$\phi(T_f^*) = \phi_f = \text{constant} \quad D(T_f^*) = D_f = \text{constant}$$

which may then be used in eq. (15) of Appendix E for partial state propagation during the "off" period.

In this way, the state variables can be propagated by constant state transition matrices until either the fixed, known T_n has elapsed, or, with the switch off, until the unknown period T_f has been transgressed. In the latter case, after exceeding the threshold, iterative linearization on the propagation time T , which appears as a parameter in the expression for the closed form solution, is used to determine the exact time when the integrator output has reached the threshold E_T . The use of the closed form solutions is very important for speeding up the simulation run-time, since otherwise, because of the low system damping and the switching discontinuity, very

small integration steps would have to be used.

A simulation program was prepared and exercised with several runs, two of which are included in this Appendix. Computer results in terms of graphs are shown in Figures A and B. The runs are comprised of a steady-state inductor current and a transient caused by a step change in the supply voltage. Agreement of the simulation results with actual laboratory test data was excellent throughout.

The digital simulation program is very efficient with respect to computation time because of the use of the closed form solution. The central processor time for Figs. A and B are, 3.5 and 17.9 seconds, respectively. For most runs the cost of machine-plotting the results exceed the central processor cost of running the simulation. A ratio of simulated real time to computer processor time can in general, however, not be given, since this depends on the granularity of the desired results, that is, how many data points for plotting are desired between switch times. But a good rule of thumb is that most runs, inclusive plotting and time-share terminal time, will cost about \$1.50 to 2.00 per run.

From the obtained results it must be concluded that a very efficient digital computer program has been written, which is easy and inexpensive to use. This demonstrates that digital computers are well suited for simulating power converter systems.

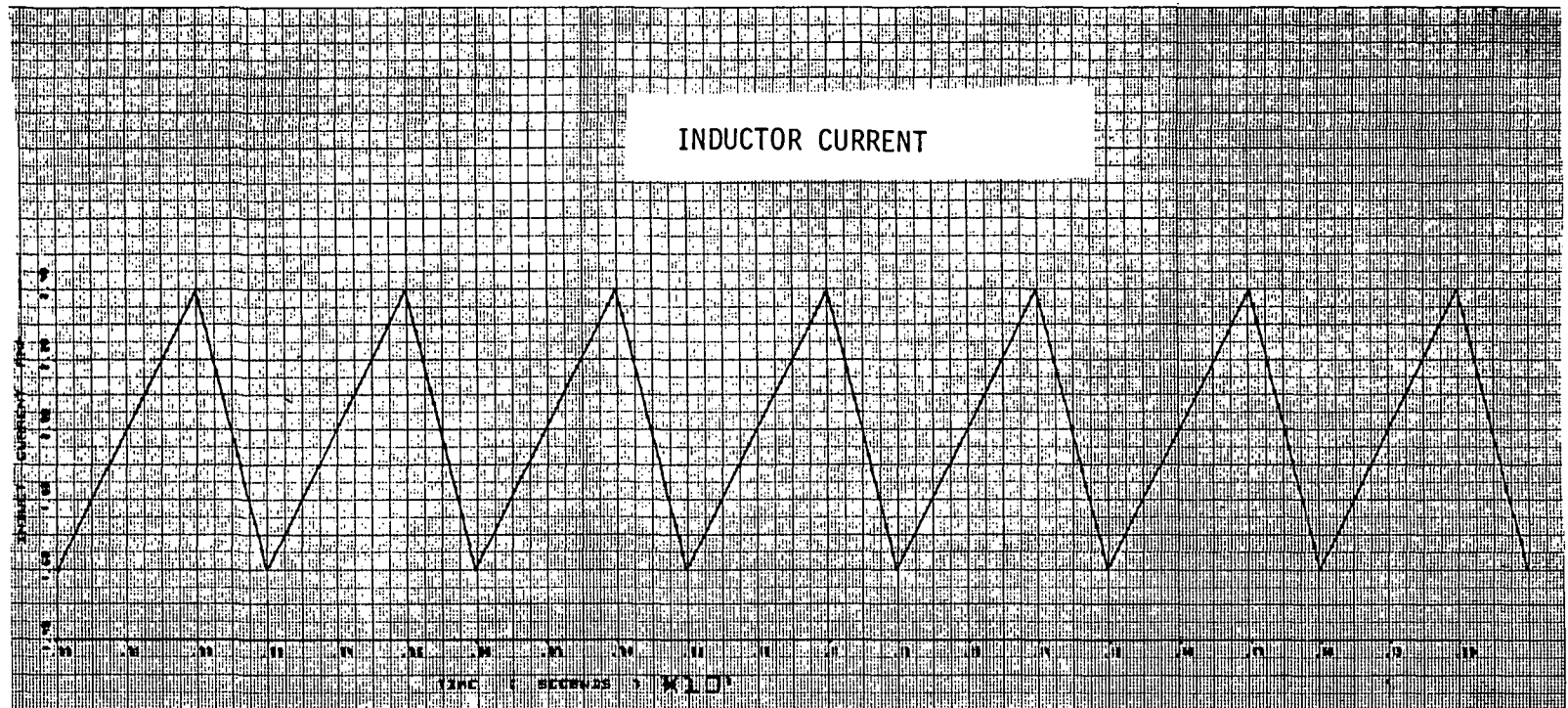


FIGURE A. WAVEFORM OF INDUCTOR CURRENT

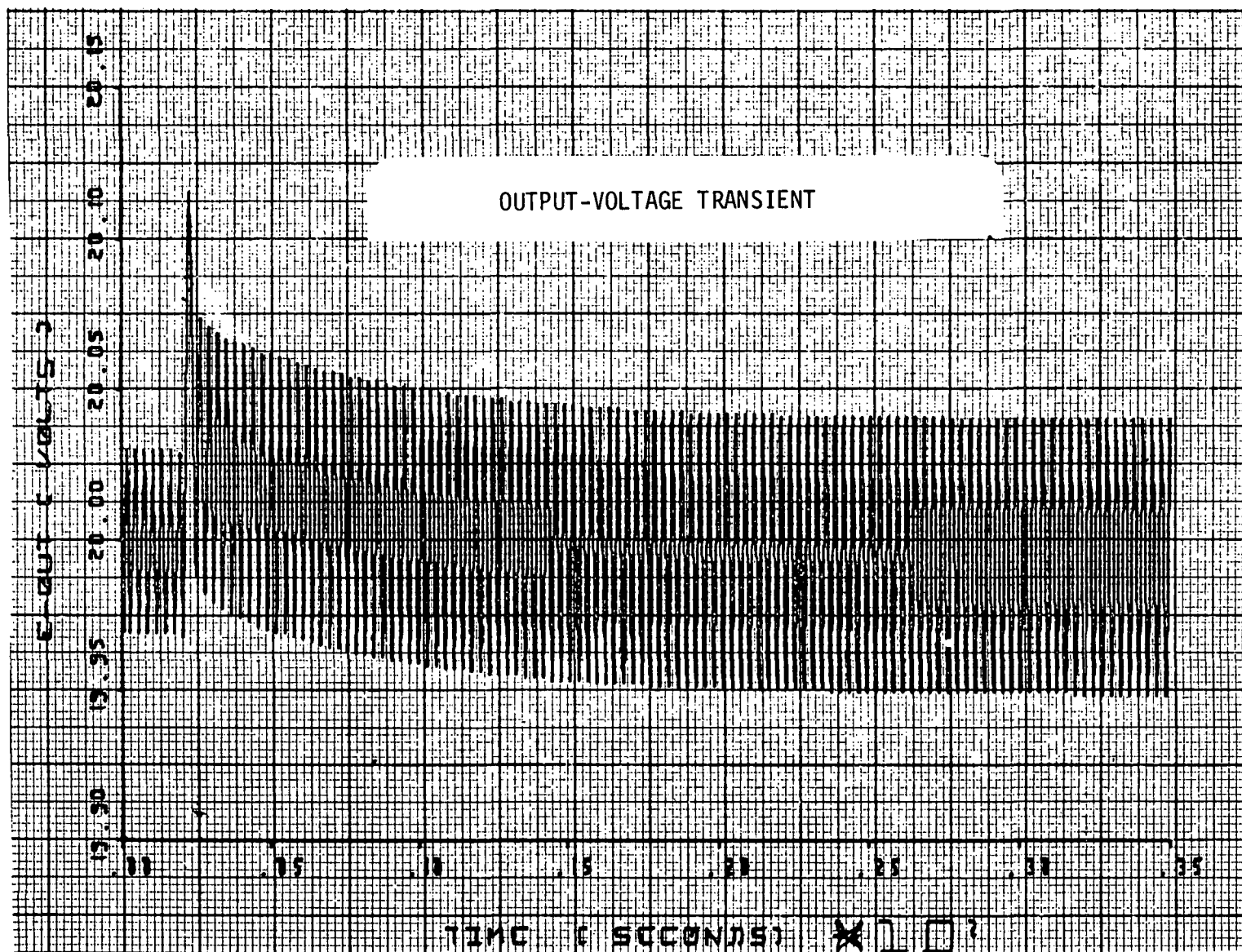


FIGURE B. REGULATOR OUTPUT-VOLTAGE TRANSIENT AS A RESULT OF STEP SUPPLY VOLTAGE CHANGE FROM 30V TO 40V

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